CHARGE-BASED MODELING OF THIN-FILM SILICON-ON-INSULATOR MOS FIELD-EFFECT TRANSISTORS

By

HYUNG-KYU LIM

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Hyung-Kyu Lim

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This dissertation describes the development of a charge-based model for thin-film SOI (Si-on-SiO_2) MOSFETs, emphasizing the structural uniqueness that distinguish them from their bulk counterparts. The SOI MOSFET, the basis of SOI and three-dimensional (3-D) MOS integrated circuits, is different because the body is thin and floating, and the underlying (back) oxide is thin enough to enable an effective back gate.

Analytic expressions for threshold voltage, drain current, and terminal charges (capacitances) of the devices in steady-state and transient conditions are derived, based on the quasi-static approximation. The modulation of the (front) channel conductance by the back-gate (substrate) bias through the completely depleted film body, and the coupling of the floating-body potential with the external voltages are explicitly accounted for in the derivation. The limiting

of the depletion-region extension by the underlying oxide simplifies the derived expressions considerably. The models are supported by comprehensive measurements of MOSFETs fabricated in recrystallized SOI films.

A charge-based large-signal model for the devices, suitable for computer simulation of transient characteristics of SOI and 3-D integrated circuits, is then developed by combining the analytic expressions. Equivalent circuits, developed from the charge-conserving model, show that the device can be accurately represented using only real reciprocal capacitances by adding a transient term in the channel transport current.

CHAPTER ONE
INTRODUCTION

Recent advances [1] in SOI (silicon-on-insulator, i.e., Si-on-SiO_2) technologies have provided viable alternatives to SOS (silicon-on-sapphire) for fabricating integrated circuits comprising advantageous dielectrically isolated devices [1,2]. Many methods to achieve thin-film SOI structures have been reported. Common ones are the recrystallization of polysilicon films deposited on silicon dioxide by laser annealing [3-5] or by graphite-strip heating [6,7], and the implantation of oxygen into single-crystal silicon [8,9].

The SOI technologies are becoming more important as CMOS (complementary metal-oxide-semiconductor) becomes the preferred technology for VLSI (very large scale integration) because of low power consumption and better compatibility with analog circuits [1]. The new SOI CMOS technology is superior to the conventional bulk technology because it eliminates latch-up, increases circuit speed by reducing parasitic capacitance, and has the flexibility to enable three-dimensional (3-D) integration [10-16]. The control of the charge condition at the back Si-SiO_2 interface by the substrate biasing is an additional advantage over the existing SOS, especially with regard to the radiation tolerance [17].

Although much emphasis has been placed on the development of the SOI fabrication technology, little work has been done on the characterization of the electrical properties of MOSFETs (metal-oxide-semiconductor field-effect-transistors) fabricated in the SOI films, which are new in structure as well as in material. In addition to the characterization of the new materials [18-21], accurate device models that account for the structural uniqueness of the devices are essential for successful development of the SOI VLSI technology.

The SOI MOSFETs, the typical structure of which we illustrate in Fig. 1.1, are different from the conventional bulk counterparts because the body is thin and floating, and the underlying (back) oxide is thin enough to enable an effective back gate. Since the SOI film body is completely depleted when the (enhancement-mode) device is ON, there is charge coupling between the front and back gates, and consequently the (front-channel) threshold voltage V_{Tf} [9,22] and the drain current I_D [23] depend on the back-gate bias V_{Gb} in the steady-state. Early studies related to this property have been carried out for the SOS MOSFET [24-26]. Since the back insulator (sapphire) is very thick for SOS devices, the studies either neglect the V_{Gb} effects [24] or only analyze the back-surface-depletion case [25]. The few studies of SOI devices that have been done are either numerical [9,22] or are not general [22].

Another important feature of the four-terminal SOI MOSFET is its floating body which causes, in addition to the "kink" in the steady-state $I_D(V_D)$ characteristic [24,27], significant deviation in the

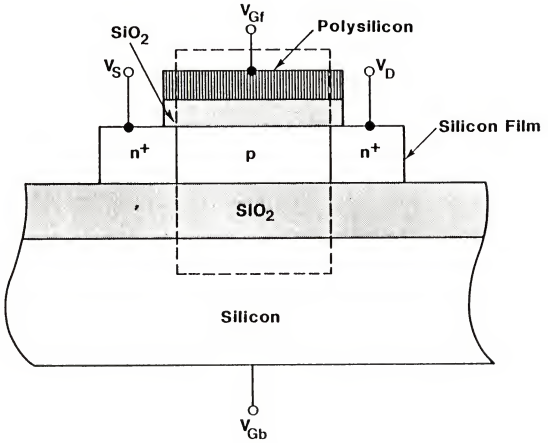

Figure 1.1 Four-terminal SOI MOSFET structure. The terminal voltages are referenced to the source voltage ($V_S = 0$). The intrinsic part of the device is enclosed by the dashed lines.

transient drain current from the corresponding steady-state value. The potential at the floating body V_B is typically deviated from zero when the device is switching because the majority carriers in the body are not supplied (or removed) freely due to the finite carrier lifetimes. This deviation causes a transient overshoot in the drain current, which in turn results in the dependence of circuit propagation delay on switching frequency. The few studies on the transient floating-body effects in SOS devices [28,29] lack quantitative treatment, and do not account for the dependence of the transient drain current on the back-gate bias, which is significant in SOI devices.

The purpose of this dissertation is to develop an accurate device model accounting for the unique features of the thin-film SOI MOSFET, which is useful for the prediction and optimization of device performance as well as for the computer-aided analysis of SOI and 3-D integrated circuits. The major contributions made in this dissertation are:

(1) the analytic characterization of threshold voltage and drain current of the thin-film SOI MOSFET in the steady state, emphasizing their dependences on V_{Gb};

(2) the modeling of the transient drain current caused by the floating-body effects and its effect on the propagation delay in SOI circuits;

(3) the development of a charge-based large-signal model of the device useful for the computer-aided transient analysis of SOI and 3-D circuits;

(4) the experimental support for the developed models by measurements of typical SOI MOSFETs and circuits fabricated in recrystallized silicon films.

The limiting of the depletion-region extension by the back oxide linearizes the relationship between the inversion charge density and surface potential. This linearization simplifies the characterization of device properties when the back-surface charge condition is uniform from source to drain. Expressions for the drain current and terminal charges are thus considerably simpler than their bulk counterparts [30-32] for typical SOI MOSFETs.

We begin in Chapter Two analysis of steady-state charge-coupling between the front and back gates by solving Poisson's equation in the depleted film body and using Gauss' theorem at the front and back $Si-SiO_2$ interfaces, at which the inversion and accumulation layers, when they exist, are approximated as charge sheets. Closed-form expressions for V_{Tf} under all possible steady-state charge conditions are then derived from the analysis, in terms of V_{Gb} and the properties of the device, including the fixed-charge and fast surface-state densities at the back $Si-SiO_2$ interface. We demonstrate that V_{Tf} varies linearly with V_{Gb} until inversion or accumulation charge at the back silicon surface blocks the field penetration from the back insulator. Measurements of linear-region drain current in laser-recrystallized SOI MOSFETs fabricated at Texas Instruments, Inc. [33] are discussed and shown to support the V_{Tf} model. A novel experimental method to evaluate

the front-gate threshold shift caused by a change in V_{Gb}, even when the back channel is conducting, is also suggested in the chapter.

The charge coupling influences the current-voltage characteristics more significantly when the drain voltage V_D is high because the back surface near the drain remains depleted for a wider range of V_{Gb}. We present in Chapter Three a simple analytic model for the strong-inversion current-voltage characteristics of the device in steady state. The dependences of I_D on V_{Gb}, V_D, and the front-gate voltage V_{Gf} for all regions of operation are explicitly shown in the derived expressions. The model is supported by extensive measurements of current-voltage characteristics of laser-recrystallized SOI MOSFETs [33]. The theoretical and experimental $I_D(V_{Gf}, V_{Gb}, V_D)$ plots show good agreement until carrier mobility degradation at high V_{Gf} causes discrepancies. The dependences of carrier mobility on terminal voltages are modeled, using the empirical model [34] for bulk MOSFET, and used to explain the discrepancies.

Transient characteristics of SOI MOSFETs are important because they determine the speed of SOI circuits [29]. In Chapter Four we model the transient overshoot in I_D after abrupt turn-ON, which occurs because the body is floating. The dependences of the overshoot on switching frequency and back-gate biasing are described by 1) expressing the saturation drain current in terms of V_B, 2) finding the relationship between V_B and the charge stored in the body, 3) modeling the time-dependence of the body charge, defined by the carrier generation and recombination in the body. Measurements of transient saturation current

in recrystallized SOI MOSFETs [33] are shown to support the analysis. The measured currents clearly show predicted dependences of the overshoot on switching frequency and on V_{Gb}. Propagation delay of CMOS inverters is measured using cascades of inverters and ring oscillators [33], and its dependences on frequency and V_{Gb} are qualitatively explained by the analysis and a simple relationship between the delay and drain current [35].

We develop in Chapter Five a charge-based large-signal model [36,37] for the thin-film SOI MOSFET, emphasizing its structural uniqueness. The model, intended for computer simulation of SOI and 3-D circuits, is based on the quasi-static approximation [30-32]. Closed-form expressions for the terminal charges, continuous throughout the regions of operation, are derived for the two representative back-surface charge conditions: accumulation and depletion. Conservation of charge [36,37] is of major concern in the partition of the channel charge into the source and drain charges. All the charging currents in the device are then defined by the time-derivatives of the derived charge expressions. An equivalent circuit for the device is also developed, from the charge-conserving model. It is shown that because of the thin-film structure, the device can be represented with only real reciprocal capacitances by incorporating all the transcapacitive current sources [38,39], which imply nonreciprocities in the MOSFET capacitances, into a transient source-drain transport current that reflects the finite carrier transit delay through the channel. The analytic expression for the transient current, which can be obtained

because of the thin-film structure, enables the evaluation of the average transit delay as well as of the charge nonconservation in the conventional reciprocal capacitance MOSFET model [30,40] that ignores the delay.

We summarize in Chapter Six the developed models and discuss their usefulness in SOI device and circuit design. Suggestions for further research are also included in the chapter.

CHAPTER TWO
THRESHOLD VOLTAGE

2.1 Introduction

The threshold voltage of a MOSFET is the onset value of the gate voltage at which a conducting channel, an inversion layer for a typical enhancement-mode device, is induced at the surface. Because of the nonlinear dependence of the inversion charge on the gate voltage, there are several ways to define the threshold voltage. A common definition used in analytic modeling of the threshold voltage is the gate voltage at which the surface potential is equal to twice the body Fermi potential ϕ_B [30-32]. Although the surface potential is higher than $2\phi_B$ by a few thermal voltages (kT/q) in strong inversion [41-43], which makes the definition not completely consistent with the experimentally determined threshold voltage we discuss later in this chapter, assuming the surface potential to be pinned at $2\phi_B$ in strong inversion simplifies the threshold voltage model while providing sufficient accuracy in the predictions of both the threshold voltage and the drain current [30-32].

In this chapter we present a general steady-state analysis of the charge coupling between the front and back gates of the SOI MOSFET that yields closed-form expressions for V_{Tf} under all possible steady-state charge conditions of the back surface. We initially assume a uniform

doping density in the silicon film, but later the analysis is extended to account for the nonuniform density resulting from a deep boron implant commonly used in the n-channel MOSFET to suppress the back-surface leakage. To render the model applicable to SOI circuit analysis, we approximate the back accumulation layer, when it exists, as a charge sheet and use the depletion approximation [30-32], the general validity of which we discuss. The results can also be applied to SOS MOSFETs by setting the back-gate insulator capacitance to zero.

The analysis yields a description of V_{Tf} in terms of the back-gate bias and the properties of the device, including those of the back Si-SiO_2 interface, i.e., the fixed-charge and fast surface-state densities. Consideration of the effect of potential drop in the silicon substrate [44] is included (Appendix A) and shown to be typically insignificant. The analysis also leads to a simple characterization of the drain current in the linear region (low drain voltage) of operation.

Results of drain current measurements of laser-recrystallized SOI MOSFETs in the linear region (low drain voltage) are discussed and shown to support the analysis. These measurements reveal, in accord with the analysis, that the back gate not only affects the back-channel conduction but also, in typical devices, can significantly affect the front-channel conduction. The results therefore indicate how well the back-gate parameters must be controlled across an SOI wafer to ensure acceptable chip yield. Furthermore they suggest how the back-gate bias may provide a control by which optimal SOI MOSFET performance in

particular applications is derived. This control does not exist in SOS MOSFETs.

2.2. Threshold Voltage of a Completely Depleted SOI MOSFET

The device we analyze is the four-terminal enhancement-mode SOI MOSFET (n-channel) illustrated in Fig. 1.1. It is fabricated in a recrystallized silicon (we ignore the grain boundaries) film on an insulating layer of silicon dioxide, which has been thermally grown or deposited on a silicon substrate. The front (polysilicon) and back (silicon substrate) gates compete for charge in the film body, which is manifested as the dependence of the (front-gate) threshold voltage on the back-gate bias and properties. Although the analysis refers directly to the device structure in Fig. 1.1, it can be applied to any MISIM device, e.g., the SOS MOSFET.

If the silicon film is sufficiently thick, it will never be completely depleted, and hence there will be no interaction, in steady-state, between the two gates. In this case, the conduction in the front as well as the back channel is described by conventional bulk MOSFET theory [30]. However the film thickness of typical SOI MOSFETs is thin enough that complete depletion can occur, thereby coupling the two gates and rendering the threshold voltage of each gate dependent on the conditions at the other. We now analyse these dependences.

To emphasize the charge coupling, we neglect small-geometry effects [45] and consider the one-dimensional active portion of the MOSFET shown in Fig. 2.1. The front (ψ_{sf}) and back (ψ_{sb}) surface potentials are the

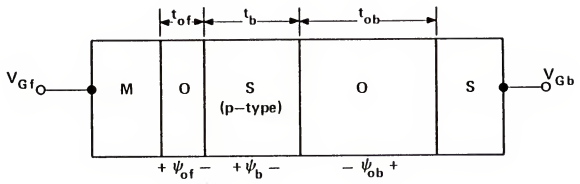

Figure 2.1 One-dimensional active portion of the SOI MOSFET. To simplify the notation, the front gate is labeled M even though it is typically polysilicon.

band bending from a hypothetical neutral film-body point to the respective surface. The electrostatic potential at this point, if the source is grounded, is just the built-in potential of the source-film body junction. Thus in analogy to bulk MOSFET theory [30], we can write

$$V_{Gf} = \psi_{sf} + \psi_{of} + \Phi^{f}_{MS} \tag{2.1}$$

and

$$V_{Gb} = \psi_{sb} + \psi_{ob} + \Phi^{b}_{MS} \tag{2.2}$$

where ψ_{of} and ψ_{ob} are the potential drops across the front- and back-gate oxides, and Φ^{f}_{MS} and Φ^{b}_{MS} are the front and back gate-body work-function differences. We have not included in (2.2) a possible potential drop in the silicon substrate (back gate) [44]. We justify this neglect later in this section. Note that the difference between (2.1) and (2.2) would follow directly by summing the potential drops between the two gates.

If the silicon film is completely depleted, except for perhaps narrow inversion or accumulation layers at the surfaces, then the charge density is $-qN_A$, and integration of Poisson's equation across the film yields

$$\psi_b \equiv \psi_{sf} - \psi_{sb} \simeq \left(E_{sf} - \frac{qt_bN_A}{2\varepsilon_s}\right) t_b \tag{2.3}$$

where E_{sf} is the electric field at the front-surface edge of the depletion region, t_b is the film thickness, and N_A is the doping density in the film, assumed for now to be uniform.

Applying Gauss' theorem to the front surface, we get

$$\psi_{of} = \frac{1}{C_{of}} (\varepsilon_s E_{sf} - Q_{ff} - Q_{cf}) \tag{2.4}$$

where $C_{of} = \varepsilon_o / t_{of}$ is the front-gate oxide capacitance, Q_{ff} is the fixed charge density at the front Si-SiO_2 interface, and Q_{cf} is the front-surface carrier charge density, which in our V_{Tf} analysis represents inversion charge. We have not explicitly in (2.4) accounted for fast surface states at the front interface since they can be implicitly accounted for by modifying Q_{ff} in a strong-inversion analysis. At the back surface,

$$-\psi_{ob} = \frac{1}{C_{ob}} (\varepsilon_s E_{sf} - qN_A t_b + Q_{fb} - qN_{sb}\psi_{sb} + Q_{cb}) \tag{2.5}$$

where $C_{ob} = \varepsilon_o / t_{ob}$, Q_{fb}, and Q_{cb} are the back-gate counterparts of C_{of}, Q_{ff}, and Q_{cf} respectively, and N_{sb} is the fast surface-state density assumed to be uniformly distributed over the energy gap. We explicitly account for N_{sb} in (2.5) because the surface-state charge will vary with V_{Gb}. In (2.5) we have implicitly expressed the electric field at the back-surface edge of the depletion region as $(E_{sf} - qN_A t_b / \varepsilon_s)$.

We relate V_{Gf} to ψ_{sf} and ψ_{sb} by combining (2.1), (2.3), and (2.4):

$$V_{Gf} = V_{FB}^{f} + (1 + \frac{C_b}{C_{of}})\ \psi_{sf} - \frac{C_b}{C_{of}}\ \psi_{sb} - \frac{Q_b/2 + Q_{cf}}{C_{of}} \qquad (2.6)$$

where $V_{FB}^{f} = \Phi_{MS}^{f} - Q_{ff}/C_{of}$ is the front-gate (bulk MOSFET) flatband voltage, $C_b = \epsilon_s/t_b$ is the depletion capacitance, and $Q_b = -qN_A t_b$ is the depletion-region areal charge density. Similarly we relate V_{Gb} to ψ_{sf} and ψ_{sb} by combining (2.2), (2.3), and (2.5):

$$V_{Gb} = V_{FB}^{b} - \frac{C_b}{C_{ob}}\ \psi_{sf} + (1 + \frac{C_b + C_{sb}}{C_{ob}})\psi_{sb} - \frac{Q_b/2 + Q_{cb}}{C_{ob}} \qquad (2.7)$$

where $V_{FB}^{b} = \Phi_{MS}^{b} - Q_{fb}/C_{ob}$ is the back-gate (bulk MOSFET) flatband voltage and $C_{sb} = qN_{sb}$. Equations (2.6) and (2.7) are the two key relations that describe the charge coupling between the front and back gates when the film body is completely depleted. Combining them leads to the description of the (front-gate) threshold voltage V_{Tf} in terms of V_{Gb} and the device parameters. We now detail the description of V_{Tf} for each possible steady-state charge condition at the back surface.

2.2.1 Accumulated Back Surface

When the back surface is accumulated, ψ_{sb} is virtually pinned at zero. Then with $\psi_{sf} = 2\phi_B$ and $Q_{cf} \simeq 0$ ($<< -Q_b$), (2.6) yields

$$V_{Tf} \simeq V_{Tf}^{A} \triangleq V_{FB}^{f} + (1 + \frac{C_b}{C_{of}})2\phi_B - \frac{Q_b}{2C_{of}} \quad . \qquad (2.8)$$

Because ψ_{sb} is virtually independent of V_{Gb} for this condition, so is V_{Tf}.

2.2.2 Inverted Back Surface

When the back surface is inverted, $\psi_{sb} \simeq 2\phi_B$. Then the threshold voltage for this case is given by (2.6) as

$$V_{Tf} \simeq V_{Tf}^I \triangleq V_{FB}^f + 2\phi_B - \frac{Q_b}{2C_{of}} \quad . \tag{2.9}$$

As is V_{Tf}^A, V_{Tf}^I is independent of V_{Gb}, again because ψ_{sb} is virtually invariant for this condition.

2.2.3 Depleted Back Surface

When the back surface is depleted, ψ_{sb} is strongly dependent on V_{Gb}; its value ranges from about zero to $2\phi_B$ between the onsets of accumulation and inversion respectively. The values of V_{Gb} (V_{Gb}^A and V_{Gb}^I) corresponding to these onsets when the front surface is inverted ($\psi_{sf} \simeq 2\phi_B$) are defined by (2.7) with $Q_{cb} \simeq 0$ ($<< -Q_b$):

$$V_{Gb}^A \simeq V_{FB}^b - \frac{C_b}{C_{ob}} 2\phi_B - \frac{Q_b}{2C_{ob}} \quad ; \tag{2.10}$$

$$V_{Gb}^I \simeq V_{FB}^b + (1 + \frac{C_{sb}}{C_{ob}}) 2\phi_B - \frac{Q_b}{2C_{ob}} \quad . \tag{2.11}$$

The dependence of V_{Tf} on V_{Gb} for $V_{Gb}^{A} < V_{Gb} < V_{Gb}^{I}$ is obtained by combining (2.6) and (2.7) to eliminate ψ_{sb} and letting $\psi_{sf} = 2\phi_B$, $Q_{cf} \simeq 0$, and $Q_{cb} \simeq 0$. The result is

$$V_{Tf} \simeq V_{Tf}^{A} - \frac{C_b\, C_{ob}}{C_{of}(C_b + C_{ob} + C_{sb})}\,(V_{Gb} - V_{Gb}^{A})$$
$$\simeq V_{Tf}^{I} - \frac{C_b\, C_{ob}}{C_{of}(C_b + C_{ob} + C_{sb})}\,(V_{Gb} - V_{Gb}^{I}) \quad . \tag{2.12}$$

The entire dependence of V_{Tf} on V_{Gb} for the SOI MOSFET (n-channel) with its film body completely depleted is plotted in Fig. 2.2. The threshold voltage is saturated at its maximum (V_{Tf}^{A}) when the back surface is accumulated for $V_{Gb} < V_{Gb}^{A}$, and decreases linearly with increasing V_{Gb} until it is saturated at its minimum (V_{Tf}^{I}) when the back surface becomes inverted at $V_{Gb} = V_{Gb}^{I}$. The discontinuities in the slope of the plot are unreal because the transitions from one surface charge condition to another are not abrupt as was implicitly assumed in the analysis. Actually the surface potential corresponding to inversion and accumulation differs from $2\phi_B$ and zero, respectively, by a few thermal voltages (nkT/q where $n \sim 5$) depending on the degree of inversion and accumulation. These differences, which can be evaluated by numerically solving Poisson's equation in the film [22], however are typically small relative to the variation in surface potential between inversion and accumulation and hence do not significantly affect the $V_{Tf}(V_{Gb})$ characteristic. This is tantamount to the fact that the effective widths of the inversion and accumulation layers (across which the nkT/q

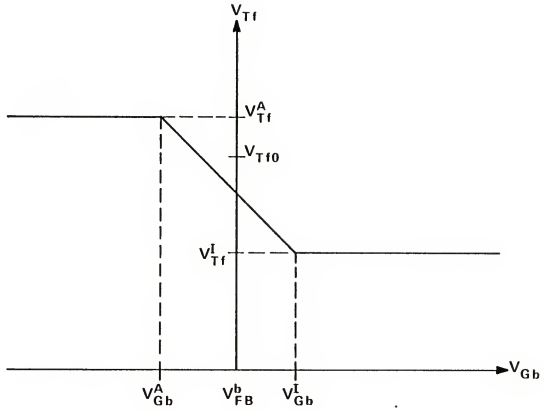

Figure 2.2 Theoretical dependence of V_{Tf} on V_{Gb} for a completely depleted SOI MOSFET. For reference, the corresponding bulk MOSFET threshold voltage V_{Tf0} is indicated.

is dropped) are typically much smaller than t_b [22], which was assumed in the derivation of (2.3).

The simplifying assumptions underlying our analysis were made to enable the derivation of closed-form expressions for V_{Tf} that could be used in an SOI MOSFET model amenable to computer-aided circuit simulation. In addition to the assumption discussed above, we also neglected in (2.2) the possible potential drop in the silicon substrate [44]. We derive in Appendix A the dependences of the substrate potential drop on V_{Gb} and device parameters. From the derivation we find that if the substrate is p-type and lowly doped ($\sim 10^{15} cm^{-3}$) and if the fixed charge densities at the silicon interfaces of the back-oxide is high ($\sim 5 \times 10^{11}$ cm^{-2}), which are typically the case [20], then for $V_{Gb}^A < V_{Gb} < V_{Gb}^I$, vis-a-vis, when V_{Tf} varies with V_{Gb}, the substrate surface is inverted, and hence the potential drop is fixed at about twice the Fermi potential of the substrate. This means that the $V_{Tf}(V_{Gb})$ characteristic in Fig. 2.2 would simply shift to the left by this drop. For typical values of t_{ob} (~ 1 μm), this drop is much less than $(V_{Gb}^I - V_{Gb}^A)$, but for thinner t_{ob} it is not. If the substrate is n-type, the surface is typically accumulated for $V_{Gb}^A < V_{Gb} < V_{Gb}^I$, and the potential drop is negligible.

2.3. General Characterization of the Threshold Voltage of SOI MOSFETs

To generalize the analysis described in Section 2.2, we must include the case of incomplete film depletion. Also the effects of nonuniform body doping, common in practical SOI MOSFETs, are worthwhile to analyze.

2.3.1 Dependences of Threshold Voltage on Film Thickness and Doping Density

We first define the conditions for which the assumption that the silicon film is completely depleted is valid. The complete-depletion condition depends on the relative values of t_b and

$$x_{d(max)} = \left[\frac{2\epsilon_s(2\phi_B)}{qN_A}\right]^{1/2} , \tag{2.13}$$

the maximum depletion-region width extending from an inverted surface in steady state [22]. In using (2.13) we are implicitly assuming that the transitions from depletion to neutrality in the film occur abruptly. Actually these transitions occur over a few Debye lengths L_D [32]. However $L_D << x_{d(max)}$, irrespective of N_A, and hence the charge in a transition region is much smaller than that in the associated depletion region. Consequently the charge coupling between the front and back gates effected by overlapping transition regions is negligible, and an analysis based on this depletion approximation is sufficiently accurate for developing SOI MOSFET models for computer-aided simulation. We consider the following three cases.

Case I: $t_b > 2x_{d(max)}$

In this case the film body can never be completely depleted by any combination of V_{Gf} and V_{Gb}. Consequently there is no charge coupling between the front and back gates in steady state, and V_{Tf} is given by the bulk MOSFET theory [32]:

$$V_{Tf} = V_{Tf0} \triangleq V_{FB}^f + 2\phi_B + \frac{qN_A x_{d(max)}}{C_{of}} . \tag{2.14}$$

Case II: $t_b < x_{d(max)}$

In this case the film body is necessarily completely depleted at the threshold condition of the front gate, irrespective of V_{Gb}. Thus V_{Tf} and its dependence on V_{Gb} are given directly by the results of Section 2.2, which are plotted in Fig. 2.2. Note that V_{Tf} can exceed V_{Tf0}. This is the case when the electric field at the back surface is sufficiently positive (same direction as E_{sf}), for example, when the back surface is accumulated. Then since the integral of the electric field over the depleted film at threshold is fixed at about $2\phi_B$, E_{sf} will increase as t_b decreases, and hence V_{Tf} can become very high.

Case III: $x_{d(max)} < t_b < 2x_{d(max)}$

In this case the depletion condition of the film body at threshold depends on V_{Gb}. To describe this dependence, we first define V_{Gb}^C as the value of V_{Gb} above which the film is completely depleted when the front surface is inverted. Recognizing that the depletion-region width extending from the back surface at $V_{Gb} = V_{Gb}^C$ is $[t_b - x_{d(max)}]$, we can write [32]

$$V_{Gb}^C = V_{FB}^b + \left(1 + \frac{C_{sb}}{C_{ob}}\right)\frac{qN_A}{2\varepsilon_s}[t_b - x_{d(max)}]^2 + \frac{qN_A}{C_{ob}}[t_b - x_{d(max)}] \quad . \tag{2.15}$$

Now for $V_{Gb} < V_{Gb}^C$, the silicon film is not completely depleted, and V_{Tf} is V_{Tf0} given by (2.14). For $V_{Gb} > V_{Gb}^C$, V_{Tf} is given by the results of Section 2.2. That is, for $V_{Gb}^C < V_{Gb} < V_{Gb}^I$, V_{Tf} is given by (2.12), and

for $V_{Gb} > V_{Gb}^I$, it is given by (2.9). As V_{Gb} increases from V_{Gb}^C to V_{Gb}^I, V_{Tf} decreases from V_{Tf0} to V_{Tf}^I.

In Fig. 2.3 we have plotted the dependences of V_{Tf} on V_{Gb} for several ratios of t_b and $x_{d(max)}$, which is fixed by N_A as described in (2.13). As expected, the sensitivity of V_{Tf} to V_{Gb} diminishes as t_b increases, and interestingly the sensitivity of V_{Tf} to t_b is reduced as V_{Gb} is decreased. We note that the dependence of V_{Tf} on V_{FB}^b ($= \phi_{MS}^b - Q_{fb}/C_{ob}$) is also given by the plots in Fig. 2.3. These plots are thus important in identifying ways to suppress the influence of Q_{fb}, which is difficult to control uniformly across an SOI wafer. As evident in Fig. 2.3 one such way is to apply a sufficiently negative V_{Gb}. The dependence of V_{Tf} on N_A is implied by Fig. 2.4 in which we have plotted V_{Tf} versus V_{Gb} for several values of $x_{d(max)}$, defined by N_A in (2.13), relative to t_b, which is fixed. We see that V_{Tf} becomes less sensitive to N_A as V_{Gb} decreases. Furthermore, as N_A decreases [vis-a-vis, $x_{d(max)}$ increases], the sensitivity of V_{Tf} to V_{Gb} is enhanced until $x_{d(max)}$ reaches t_b.

2.3.2 Deep-Boron-Implanted Film Body

It is common in the fabrication of n-channel SOI MOSFETs to implant boron deep into the film body so as to avoid depletion or inversion at the back surface [46]. This implant serves to suppress the back-surface leakage current as well as to negate the dependence of the front-channel conduction on the back-gate parameters, e.g., Q_{fb}.

To account for this implant in our analysis, we approximate the resultant nonuniform doping density $N_A(x)$ by a step profile as shown in

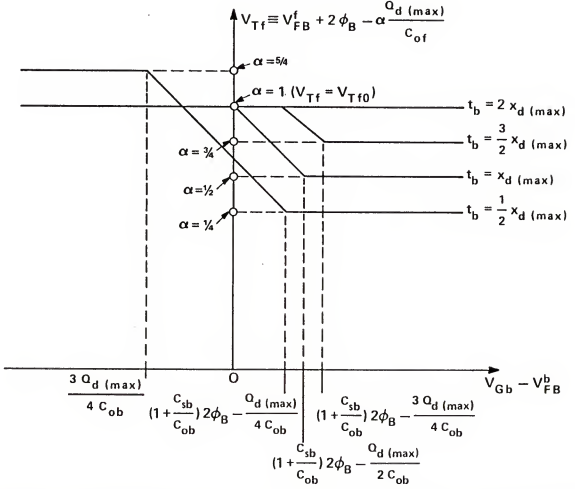

Figure 2.3 Theoretical dependences of V_{Tf} on V_{Gb} and t_b for the four-terminal SOI MOSFET with fixed N_A, which defines $x_{d(max)}$ and $Q_{d(max)} = -qN_A x_{d(max)}$. The parameter α is used to simplify the scaling of the V_{Tf} axis.

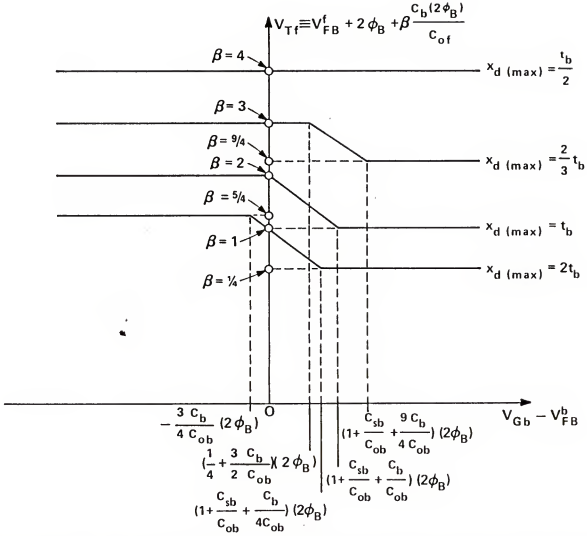

Figure 2.4 Theoretical dependences of V_{Tf} on V_{Gb} and N_A [through $x_{d(max)}$] for the four-terminal SOI MOSFET with fixed t_b. The parameter β is used to simplify the scaling of the V_{Tf} axis. Note that θ_B, which depends on N_A, varies slightly from one curve to another.

Fig. 2.5. For the case of interest in which the depletion region from the inverted front surface extends to the implanted region [$t_s < x_{d(max)}$], but not to the back surface, the charge distribution and the electric field and electrostatic potential variations in the film body are as illustrated in Fig. 2.5. The threshold voltage of the n-channel MOSFET in this case is

$$V_{Tf} = V_{FB}^{f} + 2\phi_B + \frac{q(N_{Af}t_s + N_{Ab}x_{di})}{C_{of}} \tag{2.16}$$

where N_{Af} and N_{Ab} are the front and back doping densities in the film body that define the step at $x = t_s$ (see Fig. 2.5) and x_{di} is the extent of the depletion into the implanted ($N_A = N_{Ab}$) region. We stress that V_{FB}^{f} includes the front gate-body work-function difference defined by $N_A = N_{Af}$, and hence implicitly accounts for the equilibrium potential barrier at $x = t_s$, $\Delta\phi_B = (kT/q)\ln(N_{Ab}/N_{Af})$. That is, when the front surface is strongly inverted, $\psi_{sf} \simeq 2\phi_B + \Delta\phi_B$ as indicated in Fig. 2.5. Integration of Poisson's equation in the depletion region gives x_{di} in terms of ψ_{sf}:

$$x_{di} = -t_s + \left[t_s^2\left(1 - \frac{N_{Af}}{N_{Ab}}\right) + \frac{2\varepsilon_s\psi_{sf}}{qN_{Ab}}\right]^{1/2} . \tag{2.17}$$

Inserting (2.17) into (2.16) then gives the desired expression for V_{Tf}.

We note that this result can be simplified in most cases because N_{Ab} ($>> N_{Af}$) is typically high enough that the square-root term in

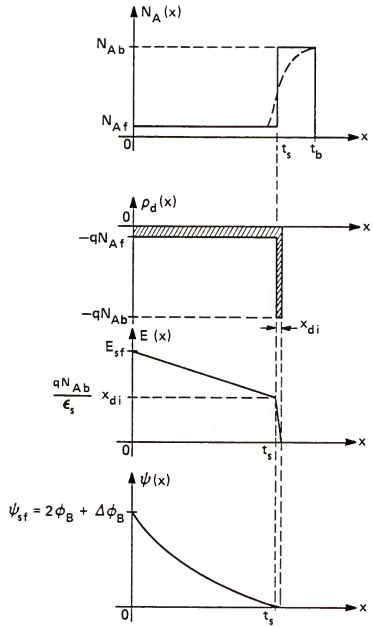

Figure 2.5 The doping density profile $N_A(x)$ and its step-function approximation for the n-channel SOI MOSFET with a deep boron implant. The charge distribution $\rho_d(x)$and the electric field E(x) and electrostatic potential $\psi(x)$ variations follow from the approximate profile when the front surface is strongly inverted and the depletion approximation is used.

(2.17) is approximated well by the first two terms of its Taylor-series expansion. Then (2.17) becomes

$$x_{di} \simeq \frac{\varepsilon_s \psi_{sf}}{q t_s N_{Ab}} - \frac{t_s N_{Af}}{2 N_{Ab}} \quad , \tag{2.18}$$

which, with (2.16) and the threshold condition $\psi_{sf} = 2\phi_B + \Delta\phi_B$, yields

$$V_{Tf} \simeq V_{FB}^f + \frac{C_{bf}}{C_{of}} \Delta\phi_B + (1 + \frac{C_{bf}}{C_{of}}) 2\phi_B - \frac{Q_{bf}}{2C_{of}} \tag{2.19}$$

where $C_{bf} = \varepsilon_s / t_s$ and $Q_{bf} = -qN_{Af}t_s$. Note the similarity between (2.19) and V_{Tf}^A defined in (2.8): except for the $\Delta\phi_B$ term, (2.19) is identical to V_{Tf}^A if t_s replaces t_b. The threshold voltage is uniquely defined by N_{Af}, N_{Ab}, t_s, and the front-gate parameters; it does not depend on the back-gate parameters.

2.4 Experimental Support and Discussion

To provide experimental support for the analysis described in this paper, we measured linear-region $I_D(V_D, V_{Gf}, V_{Gb})$ characteristics of four-terminal SOI MOSFETs (n-channel) fabricated at Texas Instruments, Inc. [33]. The silicon film is 0.5 μm thick and was laser-recrystallized after being deposited on a 1-μm-thick layer of silicon-dioxide ($C_{ob} \simeq 3.5 \times 10^{-9}$ F/cm^2), which had been thermally grown on a p-type silicon substrate with resistivity of 6-8 Ω-cm. The film was doped by ion implantation that yielded, based on SUPREME-II calculations [33], $N_A \simeq 2 \times 10^{16}$ cm^{-3} near the front surface and

$N_A \approx 10^{15}$ cm^{-3} at the back surface. No deep boron implant was done. The front gate is n^+ polysilicon, and the gate oxide thickness is 600 Å ($C_{of} \approx 5.8 \times 10^{-8}$ F/cm^2). Large devices (Z = L = 40 μm) were selected to avoid unnecessary complications, e.g., small-geometry effects [45].

For strong-inversion conditions in the linear region [$V_D << (V_{Gf} - V_{Tf})$], I_D is approximately related to V_{Tf} by [32]

$$I_D \approx \frac{Z}{L} \mu_{nf} C_{of} (V_{Gf} - V_{Tf}) V_D \tag{2.20}$$

where the terms have their usual meanings. We note that V_{Tf} in (2.20), which is the threshold voltage implied by the linear extrapolation of the measured $I_D(V_{Gf})$ characteristic to the V_{Gf} axis, is not exactly the threshold voltage we defined in Section 2.3, but is typically ~ 0.1 V higher [43]. This difference, which reflects the difference between ψ_{sf} and $2\phi_B$, is however not strongly dependent on V_{Gb}, and hence (2.20) can be used in conjunction with our measurements to check our theoretical predictions for $V_{Tf}(V_{Gb})$.

If the back-channel current I_{BC} is significant, it must be added to (2.20):

$$I_D + I_D + I_{BC} \quad . \tag{2.21}$$

Note that I_{BC} could be expressed in the form of (2.20) with the back-gate parameters and voltage substituted for μ_{nf}, C_{of}, V_{Tf}, and V_{Gf}. The back-gate counterpart to V_{Tf} could further be characterized as was V_{Tf} using the analysis described in Sections 2.2 and 2.3.

Because of I_{BC} and its dependence on V_{Gf} implied by our analysis, V_{Tf}^{I} cannot be determined from the direct extrapolation of (2.20) with sufficient accuracy to measure the dependence of V_{Tf} on V_{Gb}. Furthermore, the conductance properties of the MOSFETs measured are influenced by grain boundaries in the laser-recrystallized (poly)silicon film. Grain-boundary scattering, which dependes on V_{Gf}, affects the channel mobility μ_{nf} in (2.20) and causes an apparent increase in V_{Tf} [21]. Thus the common measurement of threshold voltage based on the extrapolation of (2.20) yields ambiguous results for these devices.

However, it is possible to detect the dependence of V_{Tf} on V_{Gb} for these devices using the experimental method we now describe. If fact, we propose this novel measurement method be generally used in the characterization of the charge coupling in thin-film MOSFET. For a given V_{Gb}, we measure

$$\Delta I_D \triangleq I_D(V_{Gf} > V_{Tf}) - I_D(V_{Gf} << V_{Tf}) \quad , \tag{2.22}$$

which is merely the change in I_D that occurs when the front-surface condition is altered from accumulation to strong inversion. Recognizing that $x_{d(max)} < t_b < 2x_{d(max)}$ in these devices and referring to Case III in Subsection 2.3.1 and to (2.20) and (2.21), we can write

$$\Delta I_D \simeq \Delta I_{D1} \triangleq g_{mf}(V_{Gf} - V_{Tf0}) \qquad \text{for } V_{Gb} < V_{Gb}^{C} \quad , \tag{2.23}$$

$$\Delta I_D \simeq \Delta I_{D2} \triangleq g_{mf}[V_{Gf} - V_{Tf}(V_{Gb})] \qquad \text{for } V_{Gb}^C < V_{Gb} < V_{Tb}^I \quad , \tag{2.24}$$

$$\Delta I_D \simeq \Delta I_{D3} \triangleq g_{mf}(V_{Gf} - V_{Tf}^I) + g_{mb}(V_{Gb} - V_{Tb}^I) \qquad \text{for } V_{Tb}^I < V_{Gb} < V_{TbO} \quad , \tag{2.25}$$

and

$$\Delta I_D \simeq \Delta I_{D4} \triangleq g_{mf}(V_{Gf} - V_{Tf}^I) + g_{mb}(V_{TbO} - V_{Tb}^I) \qquad \text{for } V_{Gb} > V_{TbO} \tag{2.26}$$

where

$$g_{mf} = \frac{Z}{L} \mu_{nf} C_{of} V_D \tag{2.27}$$

and where g_{mb}, V_{Tb}^I, and V_{TbO} are the back-gate counterparts of g_{mf}, V_{Tf}^I, and V_{TfO} respectively. The expressions for the back-gate threshold voltage, however, should include the back surface-state charging term $[(C_{sb}/C_{ob})2\phi_B]$. We have neglected the grain-boundary effects on channel conductance, which are significant only for relatively low values of V_{Gf} [21].

We see from (2.23) and (2.26) that at a fixed V_{Gf}, ΔI_D is independent of V_{Gb} when V_{Gb} is sufficiently low ($< V_{Gb}^C$) or sufficiently high ($> V_{TbO}$). When $V_{Gb}^C < V_{Gb} < V_{Tb}^I$, (2.24) shows that ΔI_D increases with increasing V_{Gb} because V_{Tf} is decreasing; whereas when $V_{Tb}^I < V_{Gb} < V_{TbO}$, (2.25) shows that it increases with V_{Gb} because of

back-channel conduction. Note then that the difference between ΔI_{D4} and ΔI_{D1} reveals quantitatively the shift in V_{Tf} resulting from the corresponding change in V_{Gb}. From (2.23) and (2.26) we have

$$\Delta I_{D4} - \Delta I_{D1} = g_{mf}(V_{TfO} - V_{Tf}^{I}) + g_{mb}(V_{TbO} - V_{Tb}^{I}) \tag{2.28}$$

$$\equiv g_{mf}(V_{TfO} - V_{Tf}^{I})(1 + \frac{\mu_{nb}}{\mu_{nf}}) \quad ; \tag{2.29}$$

the equivalent expression (2.29) follows from (2.28) when we note from (2.9) and (2.14) that

$$V_{TfO} - V_{Tf}^{I} = \frac{qN_A}{C_{of}}[x_{d(max)} - \frac{t_b}{2}] \quad , \tag{2.30}$$

and hence that $(V_{TbO} - V_{Tb}^{I})$ can be expressed similarly. Thus if μ_{nf} and μ_{nb} are known, then measuring $(\Delta I_{D4} - \Delta I_{D1})$ implies, via (2.29), $(V_{TfO} - V_{Tf}^{I})$, which reflects the influence of V_{Gb} on V_{Tf}. Note that this experimental development can be used for $t_b < x_{d(max)}$ case also, by simply replacing V_{TfO}, V_{Tbo}, and V_{Gb}^{C} with V_{Tf}^{A}, V_{Tb}^{A}, and V_{Gb}^{A} respectively.

We have plotted in Fig. 2.6 the measured dependence of ΔI_D on V_{Gb}, which resulted when $V_{Gf} = \pm 1$ V was used to invert and accumulate the front surface. As predicted by our analysis, ΔI_D saturates when V_{Gb} is sufficiently low or high. For comparison we plot also in Fig. 2.6 the calculated (estimated) $\Delta I_D(V_{Gb})$ dependence obtained from (2.23)-(2.27). For the calculations, g_{mf} and g_{mb} were <u>estimated</u> from linear-region

$I_D(V_{Gf},V_{Gb})$ measurements, and V_{Tf} and V_{Tb} were evaluated using our analysis, the same measurements, and estimated device parameter values [33]. The fact that the theoretical and experimental curves in Fig. 2.6 have the same basic shape supports our analysis. We note that the fast surface states at the back Si-SiO_2 interface ($N_{sb} \approx 3 \times 10^{11}$ cm^{-2}/eV [33]) stretch-out the $\Delta I_D(V_{Gb})$ curve along the V_{Gb} axis. This stretch-out, which is described by ΔI_{D2}, reflects variation in the charge of the surface states resulting from change in V_{Gb}, i.e., in ψ_{sb}.

An obvious discrepancy between the calculated and measured results plotted in Fig. 2.6 is the difference between the respective values of $(\Delta I_{D4}-\Delta I_{D1})$. This difference implies a discrepancy between our theoretical and experimental estimations of $(V_{Tf0} - V_{Tf}^I)$ based on (2.30) and (2.29) respectively. The measurements yield 0.21 V whereas the theory predicts 0.14 V. Because the grain boundaries tend to reduce I_D [21], they are probably not the cause of this discrepancy. More plausible reasons are the nonuniform $N_A(x)$ and/or uncertainty in t_b. Assuming about a 10%-thinner t_b will remove the discrepancy.

The theoretical and experimental results plotted in Fig. 2.6 imply that in typical SOI MOSFETS the charge condition of the back surface, which is defined by V_{Gb} and the properties of the Si-SiO_2 interface, can significantly affect the conduction properties of the front surface, and vice versa. We note that the back-gate influence on I_D is even stronger for thinner silicon films and for lower doping densities in the film as implied by Figs. 2.3 and 2.4.

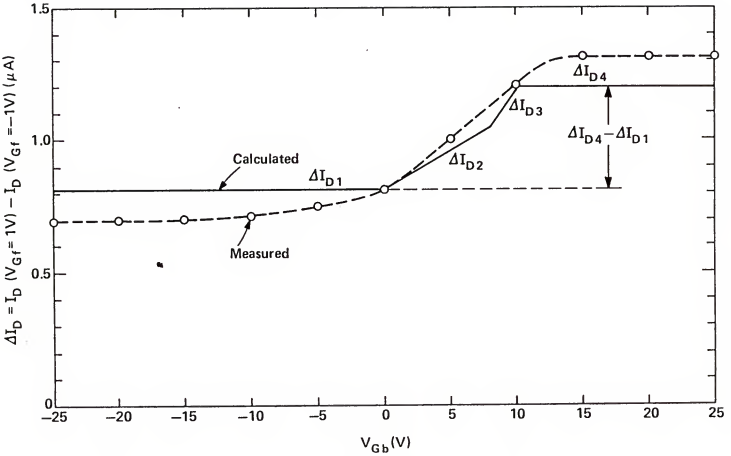

Figure 2.6 Calculated and measured ΔI_D versus V_{Gb} for a four-terminal laser-recrystallized SOI MOSFET reflecting the dependence of V_{Tf} on V_{Gb}.

The variations in V_{Tf} and I_D discussed above, which result from changes in the back-surface charge condition, can be induced by variations in V_{FB}^b, i.e., Q_{fb}, as well as in V_{Gb}. Hence the results indicate how well Q_{fb} must be controlled across an SOI wafer to ensure acceptable chip yield. To exemplify further the sensitivity of V_{Tf} to Q_{fb}, we note from (2.12), when V_{Gb} is fixed such that the film body is completely depleted (e.g., V_{Gb} = 0 for the devices used in our measurements), that

$$\frac{dV_{Tf}}{dQ_{fb}} \cong \frac{-C_b}{C_{of}(C_b + C_{ob} + C_{sb})} \quad . \tag{2.31}$$

Hence for the devices measured, in which C_{sb} is significant, $dV_{Tf}/d(Q_{fb}/q) \cong 0.08 \times 10^{-11}$ V-cm^2. Consequently variations in (Q_{fb}/q) larger than 10^{11} cm^{-2} produce considerable changes in V_{Tf}. As evidenced by (2.31), this sensitivity is more pronounced in devices with thinner t_b but becomes less significant with increasing N_{sb}.

In most cases the sensitivity of I_D to the back-gate properties is undesirable, and processes like a deep-boron implant in the n-channel MOSFET are used to suppress it. However, there may be applications in which the front-back-gate charge coupling can be exploited to improve the MOSFET performance. As indicated in Fig. 2.2 it is possible to bias the back gate ($V_{Gb} \cong V_{Tb}^I$) such that V_{Gf} can simultaneously turn the back and front channels on and off. In this case, when the device is on ($V_{Gf} > V_{Tf}^I$), I_D is enhanced by I_{BC} as well as by an effective reduction in V_{Tf} due to V_{Gb}, which increases the front-channel conduction. When the

device is off ($V_{Gf} << V_{Tf}^{I}$), the leakage is low because V_{Tb} is increased above V_{Tb}^{I}, which implies that the back channel is off. The front-channel leakage is thus concomitantly further reduced because of an effective increase in V_{Tf}.

2.5 Summary

The charge coupling between the front and back gates of thin-film uniformly doped SOI MOSFETs has been analyzed, and closed-form expressions for the threshold voltage V_{Tf} under all possible steady-state conditions have been derived. The expressions clearly show the dependence of channel conductance in the linear region on the back-gate bias V_{Gb} and on the device parameters, including the fixed charge density Q_{fb} and the fast surface-state density N_{sb} at the back $Si\text{-}SiO_2$ interface. The threshold voltage of an n-channel SOI MOSFET having a deep boron implant that negates the influence of the back gate was also described.

The analysis, which characterizes directly the linear-region (strong inversion) drain current I_D, was supported in essence by measurements of this current in laser-recrystallized SOI MOSFETs [33]. Although the $V_{Tf}(V_{Gb})$ dependence cannot be measured directly, measurements of changes in I_D produced by variations in V_{Gb} yielded results that are basically in agreement with the theoretical predictions. This novel experimental method can be generally used to characterize $V_{Tf}(V_{Gb})$ of thin-film SOI MOSFETs.

An n-channel MOSFET was assumed in the analysis, but the corresponding results for p-channel MOSFETs can be easily derived analogously. Hence the analysis can provide a basis for optimizing the performance of SOI CMOS integrated circuits. For example, it describes how a negative V_{Gb}, despite reducing the current-drive capability in n-channel MOSFETs, could be used to diminish the sensitivity of V_{Tf} to Q_{fb} and to the silicon film parameters, e.g., thickness, all of which may vary considerably across an SOI wafer. Alternatively it describes how a deep boron implant could provide the same desensitization, thus enabling the use of V_{Gb} to optimize the performance of the p-channel MOSFET. The analysis indicated also that the current-drive capability of the SOI MOSFET could possibly be enhanced without significant increase in leakage by proper choice of V_{Gb}.

CHAPTER THREE
CURRENT-VOLTAGE CHARACTERISTICS IN STRONG INVERSION

3.1 Introduction

The current-voltage model of the MOSFET is of primary importance in the design of MOS circuits. The generalized rigorous description of I_D is extremely complex as seen in the Pao-Sah model [47], in which the drift and diffusion of carriers in the finite-thickness inversion region are described by a double-integral formula. A significant mathematical simplification of the model is achieved, without significant loss of accuracy, by assuming the inversion layer is a "charge sheet," i.e., a conducting sheet of zero thickness [48]. The model is further simplified when the device is in strong inversion since the electrochemical potential gradient along the channel, which defines the channel current, is close to the electrostatic one, and hence the carriers in the channel flow predominantly by drift [47-50]; the carrier diffusion, which is the predominant conduction echanism in weak inversion, can be ignored.

In this chapter we present a simple analytic model for the strong-inversion steady-state current-voltage characteristics of four-terminal thin-film SOI MOSFETs. The dependence of I_D on V_{Gf}, V_{Gb}, and V_D for all

regions of operation is explicitly shown in the derived expressions. Simplification of the model is achieved by recognizing, based on physical insight, that the inversion charge density anywhere in the channel can be approximated well by a linear function of the surface potential for a typical device. We assume a constant carrier mobility in the channel and a uniform doping density in the silicon film, but we include comprehensive discussions of the limitations implied by these assumptions. Because of the linearity, the model yields expressions for I_D that are simpler than those of bulk MOSFETs. The physical model can be useful in the engineering design of SOI devices and may imply optimal back-gate biases in particular SOI integrated circuits. It can also provide the basis for MOSFET models needed in computer-aided analysis of SOI MOS circuits.

Results of extensive current-voltage measurements of laser-recrystallized SOI MOSFETs are discussed and shown to support the model. Theoretical-experimental plots of $I_D(V_{Gf},V_{Gb},V_D)$ show good agreement until mobility degradation at high V_{Gf} causes discrepancies. The carrier mobility, which can be modeled similarly to that in the bulk MOSFET in the linear region, is strongly dependent on the back surface charge condition in the saturation region. The mobility degradation is most severe when the back surface is accumulated.

The model reveals that, for given values of V_{Gf} and V_D, I_D decreases as V_{Gb} is varied to change the charge condition of the back surface from depletion everywhere between the source and drain regions to accumulation everywhere. This decrease occurs because the front

inversion charge density decreases as V_{Gb} raises the electric field in the silicon film. Heavy accumulation at the back surface, for high V_D, suppresses I_D significantly because the high electric field degrades the mobility in addition to decreasing the inversion charge density. Also because of the change in the electric field, the drain saturation voltage decreases (linearly with V_{Gb}) as the back surface is biased from depletion to accumulation.

3.2 Analysis

In the derivation of expressions for $I_D(V_{Gf},V_{Gb},V_D)$, we use the common assumptions used for the bulk MOSFET in strong inversion [32]: constant mobility, long channel (gradual-channel approximation), uniform doping, and negligible diffusion current. For a strongly inverted n-channel MOSFET, the current at an arbitrary point y in the (front) channel ($0 < y < L$) is [32]

$$I(y) = Z \mu_{nf} \left|Q_n(y)\right| \frac{d\psi_{sf}(y)}{dy} \tag{3.1}$$

where $Q_n(y)$ is the inversion (electron) charge density, and μ_{nf} is the electron mobility in the channel. Integration of (3.1) from source (y=0) to drain (y=L) yields

$$I_D = \frac{Z}{L} \mu_{nf} \int_{2\phi_B}^{2\phi_B + V_D} |Q_n(y)| \, d\psi_{sf}(y) \tag{3.2}$$

where the limits $\psi_{sf}(0) = 2\phi_B$ and $\psi_{sf}(L) = 2\phi_B + V_D$ are the commonly assumed strong-inversion conditions [32].

The expression for $|Q_n(y)|$ can be obtained from the one-dimensional charge-coupling analysis in Chapter Two. With the gradual-channel approximation [32], we can extend (2.6) and (2.7) to arbitrary y at which the silicon film is comletely depleted. Then recognizing that Q_n is the Q_{cf} in (2.6), we get

$$|Q_n(y)| = C_{of} \left[V_{Gf} - V_{FB}^f - \left(1 + \frac{C_b}{C_{of}}\right)\psi_{sf}(y) + \frac{C_b}{C_{of}} \psi_{sb}(y) + \frac{Q_b}{2C_{of}} \right] \tag{3.3}$$

where

$$\psi_{sb}(y) = \frac{C_{ob}}{C_{ob} + C_b} \left[V_{Gb} - V_{FB}^b + \frac{C_b}{C_{ob}} \psi_{sf}(y) + \frac{Q_b}{2C_{ob}} + \frac{Q_{cb}(y)}{C_{ob}} \right] \tag{3.4}$$

In (3.4) we assumed a negligibly small surface-state density at the back Si-SiO_2 interface. As shown in the analysis in Chapter Two, presence of the surface states will stretch-out the $I_D(V_{Gb})$ characteristic, weakening the sensitivity of the front-channel conductance to V_{Gb}.

If the silicon film is sufficiently thick $[t_b > x_{d(max)}]$, as we have discussed in Subsection 2.3.1, it can be only partially depleted, which renders (3.3) and (3.4) not strictly valid. At points where this is the case, $Q_n[\psi_{sf}(y)]$ is given by the bulk MOSFET theory [32], and I_D in (3.2) is derived by appropriately using it or (3.3) and (3.4) as determined by $\psi_{sf}(y)$ [23]. Because $Q_n[\psi_{sf}(y)]$ is nonlinear where the film is not completely depleted, this derivation yields extremely complicated results. Simpler but sufficiently accurate results for typical SOI MOSFETs are obtained by using the linear $Q_n[\psi_{sf}(y)]$ given by (3.3) and (3.4) irrespective of whether or not a neutral region exists under part of the channel. We discuss in Appendix B the physical basis for this approximation and show that it typically results in less than 5% error in I_D provided the film is completely depleted at the drain, which usually obtains in normal operation. Thus we develop our $I_D(V_{Gf},V_{Gb},V_D)$ model based on (3.3) and (3.4), i. e., $t_b < x_{d(max)}$, but we note that it is generally applicable.

3.2.1 Possible Charge Conditions at the Back Surface

We first define the values of V_{Gb} corresponding to the onsets of back-surface accumulation and inversion at the source and drain. At sufficiently low (negative) values of V_{Gb}, the back surface is accumulated everywhere from source to drain. As V_{Gb} is increased, eventually, at $V_{Gb} = V_{Gb}^{A}(L)$, the back surface at the drain becomes depleted as implied by (3.4). The depletion of the back surface begins from the drain because $E_{sb}(y)$, the back-surface counterpart of $E_{sf}(y)$,

is high at the drain corresponding to the high $\psi_{sf}(y)$. From (3.4) with $\psi_{sf}(L) = V_D + 2\phi_B$, $\psi_{sb}(L) = 0$, and $Q_{cb}(L) = 0$,

$$V_{Gb}^{A}(L) = V_{Gb}^{A} - \frac{C_b}{C_{ob}} V_D \quad . \tag{3.5}$$

If the device is saturated, V_D in (3.5) must be replaced by $V_{D(sat)}^{A}$, the saturation drain voltage, which will be defined in Subsection 3.2.2. As V_{Gb} is increased above $V_{Gb}^{A}(L)$, the depleted portion of the back surface expands toward the souce until, at $V_{Gb} = V_{Gb}^{A}$, the back surface is completely depleted. As V_{Gb} is increased above V_{Gb}^{A}, the back surface remains depleted until V_{Gb} reaches V_{Gb}^{I}, at which the back surface becomes inverted. We illustrate in Fig. 3.1 these bias-dependent charge conditions at the back surface.

3.2.2 Expressions for the Drain Current

Combining (3.2), (3.3), and (3.4), we obtain simplified expressions for I_D in terms of V_{Gf}, V_{Gb}, and V_D for the various back surface charge conditions described in Subsection 3.2.1. We do not analyze the case in which the back surface is inverted: in practical applications it is avoided to keep the leakage current low.

Case A: Back Surface Accumulated from Source to Drain $[V_{Gb} < V_{Gb}^{A}(L)]$

When the back surface is everywhere accumulated, $\psi_{sb}(y)$ is virtually pinned at zero. Then combining (3.2) and (3.3), we get

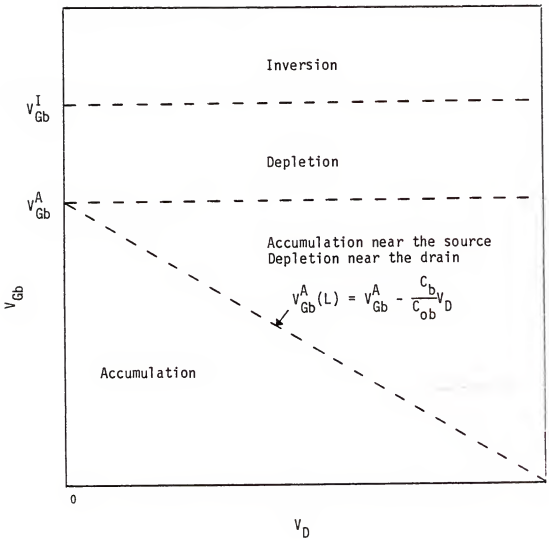

Figure 3.1 Dependences of the back-surface charge condition on V_{Gb} and V_D.

$$I_D = I_D^A \triangleq \frac{Z}{L} \mu_{nf} C_{of} \left[(V_{Gf} - V_{Tf}^A) V_D - (1 + \frac{C_b}{C_{of}}) \frac{V_D^2}{2} \right] \tag{3.6}$$

As is evident in (3.6), I_D^A does not depend on V_{Gb} because the accumulated charge prohibits modulation by V_{Gb} of the electric field in the silicon film.

The drain voltage $V_{D(sat)}$ at which the drain current saturates is obtained from [48]

$$\left. \frac{\partial I_D}{\partial V_D} \right|_{V_D = V_{D(sat)}} = 0 \quad . \tag{3.7}$$

Combining (3.6) and (3.7), we obtain

$$V_{D(sat)} = V_{D(sat)}^A \triangleq \frac{V_{Gf} - V_{Tf}^A}{1 + C_b/C_{of}} \quad . \tag{3.8}$$

The saturated drain current $I_{D(sat)}$ is obtained by evaluating (3.6) at $V_D = V_{D(sat)}^A$:

$$I_{D(sat)} = I_{D(sat)}^A \triangleq \frac{Z}{L} \frac{\mu_{nf} C_{of}}{2(1 + C_b/C_{of})} (V_{Gf} - V_{Tf}^A)^2 \quad . \tag{3.9}$$

We note that although (3.6) and (3.9) resemble corresponding approximate expressions for the bulk MOSFET [32], they are exact for the thin-film SOI MOSFET. They are simplified in this case because Q_n in (3.3) varies linearly with ψ_{sf}.

Case B: Back Surface Depleted from Source to Drain $[V_{Gb}^A < V_{Gb} < V_{Gb}^I]$

When the back surface is everywhere depleted, $Q_{cb}(y) = 0$, and (3.2), (3.3), and (3.4) yield

$$I_D = I_D^D \triangleq \frac{Z}{L} \mu_{nf} C_{of} [(V_{Gf} - V_{Tf})V_D - (1 + \frac{C_{bb}}{C_{of}}) \frac{V_D^2}{2}] \tag{3.10}$$

where the effective body capacitance $C_{bb} \triangleq \frac{C_{ob}C_b}{C_{ob} + C_b}$ is the series combination of C_b and C_{ob}, and V_{Tf} is defined in (2.12) with $C_{sb} = 0$. In this case, as we see from (3.10) and (2.12), I_D increases with increasing V_{Gb} because V_{Tf} decreases.

Using (3.7) and (3.10), we obtain

$$V_{D(sat)} = V_{D(sat)}^D \triangleq \frac{V_{Gf} - V_{Tf}}{1 + C_{bb}/C_{of}} \quad , \tag{3.11}$$

which when inserted into (3.10) gives

$$I_{D(sat)} = I_{D(sat)}^D \triangleq \frac{Z}{L} \frac{\mu_{nf} C_{of}}{2(1 + C_{bb}/C_{of})} (V_{Gf} - V_{Tf})^2 \quad . \tag{3.12}$$

Note that the resulting expressions for this case are identical to those for Case A but with V_{Tf}^A and C_b replaced by V_{Tf} and C_{bb} respectively.

Case C: Back Surface Accumulated Near Source and Depleted Near Drain $[V_{Gb}^A(L) < V_{Gb} < V_{Gb}^A]$

When V_D is high, the back surface can be depleted near the drain even though it remains accumulated near the source. If such a

transition in the charge condition of the back surface occurs at $y = y_t$, (3.2) must be rewritten as

$$I_D = \frac{Z}{L}\mu_{nf}\Big[\int_{2\phi_B}^{\psi_{sf}(y_t)} |Q_n(y)|_{\psi_{sb}(y)=0} d\psi_{sf}(y)$$

(3.13)

$$+ \int_{\psi_{sf}(y_t)}^{2\phi_B+V_D} |Q_n(y)|_{Q_{cb}(y)=0} d\psi_{sf}(y)\Big] \quad ;$$

$\psi_{sf}(y_t)$ is given by (3.4) with $\psi_{sb}(y_t) \simeq 0$ and $Q_{cb}(y_t) \simeq 0$:

$$\psi_{sf}(y_t) \simeq 2\phi_B + \frac{C_{ob}}{C_b}(V_{Gb}^A - V_{Gb}) \quad . \tag{3.14}$$

Combining (3.13) and (3.14) yields

$$I_D = I_D^{AD} \triangleq \frac{Z}{L}\mu_{nf}C_{of}\Big[(V_{Gf} - V_{Tf}^A)V_D - (1 + \frac{C_{bb}}{C_{of}})\frac{V_D^2}{2} - \frac{C_{bb}}{C_{of}}V_D(V_{Gb}^A - V_{Gb})$$

$$+ \frac{C_{bb}}{2C_{of}}\frac{C_{ob}}{C_b}(V_{Gb}^A - V_{Gb})^2\Big] \quad . \tag{3.15}$$

Note that I_D^{AD} increases with increasing V_{Gb} because y_t decreases, i.e., more of the back surface becomes depleted, and hence the dependence defined in Case B becomes more prevalent.

From (3.7) and (3.15), we get

$$V_{D(sat)} = V_{D(sat)}^{AD} \triangleq \frac{V_{Gf} - V_{Tf}^{A} - \frac{C_{bb}}{C_{of}}(V_{Gb}^{A} - V_{Gb})}{1 + C_{bb}/C_{of}} \tag{3.16}$$

and

$$I_{D(sat)} = I_{D(sat)}^{AD} \triangleq \frac{Z}{L}\frac{\mu_{nf}C_{of}}{2(1 + C_{bb}/C_{of})}\left[(V_{Gf} - V_{Tf}^{A})^{2} - 2\frac{C_{bb}}{C_{of}}(V_{Gf} - V_{Tf}^{A})(V_{Gb}^{A} - V_{Gb}) + \frac{C_{ob}}{C_{of}}\frac{C_{bb}}{C_{fb}}(V_{Gb}^{A} - V_{Gb})^{2}\right] \tag{3.17}$$

where $C_{fb} \triangleq \frac{C_{of}\,C_{b}}{C_{of} + C_{b}}$ is the series combination of C_{of} and C_{b}. Because $V_{D(sat)}$ is defined by the back-surface charge condition at the drain, (3.16) is identical to (3.11). We note that the results of this case reduce to those of Cases A and B when V_{Gb} equals $V_{Gb}^{A}(L)$ and V_{Gb}^{A} respectively.

3.3 Experimental Support and Discussion

To provide experimental support for the analysis, we measured current-voltage characteristics of four-terminal SOI MOSFETs (n-channel) described in Section 2.4.

These devices differ in three ways from the device on which the analysis in Section 3.2 is based. First, they have grain boundaries in the (poly)silicon film body, which at relatively low V_{Gf} affect the channel conductance [21]. At high enough V_{Gf} (>2 V) however, the grain-boundary effects are negligible. Second, the doping density in the film body is not uniform. Although this nonuniformity affects the $V_{Tf}(V_{Gb})$

dependence, it does not significantly affect the current-voltage characteristics well above threshold as indicated in Section 3.2. (C_b and C_{bb} are not affected by the doping profile). Third, for V_{Gb} sufficiently negative, e.g., when the back surface is accumulated, the film body is not completely depleted for low V_D, especially near the source. To account for incomplete depletion analytically is quite tedious as shown in [23], but, as we demonstrate in Appendix B, our simplified model is valid for these devices.

We plot in Fig. 3.2 the measured and calculated $I_D(V_D)$ characteristics of a representative device with V_{Gf} = 4 V and 6 V and V_{Gb} = 0 V and -80 V. The values of V_{Gb} were selected, based on measured $I_D(V_{Gb})$ characteristics, to deplete and accumulate, respectively, the entire back surface. We found from $I_D(V_{Gb})$ in the linear and saturation regions that $V_{Gb}^I \approx 0$ V and $V_{Gb}^A(L) > -80$ V respectively. For the calculation of I_D, the threshold voltages [$V_{Tf}^A \approx 0.3$ V, $V_{Tf}(V_{Gb} = 0\ V) \approx 0.1$ V] and the (maximum) electron mobility ($\mu_{nf} \approx 420\ cm^2/V\text{-sec}$) were determined from the measured $I_D(V_{Gf})$ in the linear region. At V_{Gf} = 4 V, we have good agreement between the measured and calculated results, except for the small "kink effect" at high V_D [24]. However at V_{Gf} = 6 V, the measured I_D is somewhat lower than the calculated I_D, especially for low V_D and at V_{Gb} = -80 V. This slight discrepancy can be explained by analyzing the dependences of μ_{nf} on the terminal voltages, which we do in Appendix C.

In Appendix C we show that the effective mobility in the linear region, μ_{lin}, is virtually independent of V_{Gb}, and $\mu_{lin}(V_{Gf})$ can be

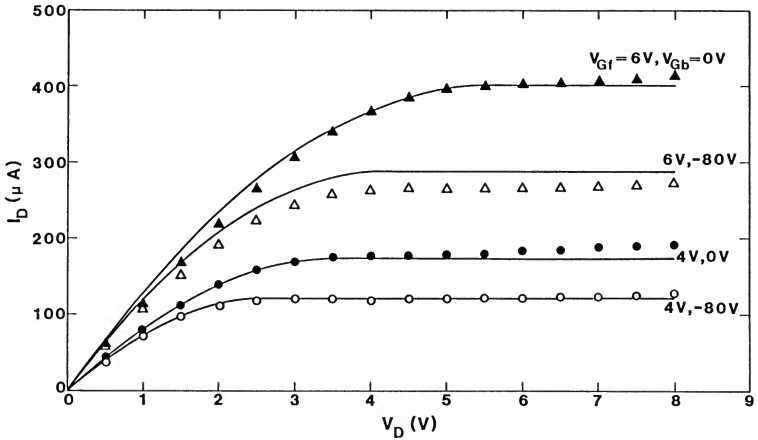

Figure 3.2 Measured (points) and calculated (curves) current-voltage characteristics of the typical SOI MOSFET described in Section 2.4.

described well using an empirical mobility model [34] developed for the bulk MOSFET. However when the device is saturated, the effective mobility μ_{sat}, which is an average value across the channel, is strongly dependent on V_{Gb}. The mobility near the drain is higher than that near the source because $|Q_n(L)| < |Q_n(0)|$ and hence the effective normal (to the surface) electric field E_{eff} in (C.2) is lower. Consequently μ_{sat} is higher than μ_{lin} and depends on V_{Gb} because $E_{eff}(L)$ does. Based on the analysis in Appendix C, we estimate that at V_{Gf} = 8 V, μ_{sat} is about 15% lower than the maximum mobility (420 cm^2/V-sec) when the back surface is depleted ($V_{Gb} \approx V_{Gb}^I$), whereas it is about 22% lower than the maximum value when the back surface is accumulated evrywhere [$V_{Gb} < V_{Gb}^A(L)$]; μ_{lin}, independent of V_{Gb}, is about 25% lower than the maximum mobility. These differences are large enough to cause the discrepancy in Fig. 3.2 noted above and those to be noted below. The mobility degradation is most severe for low V_D and/or when the back surface is accumulated.

The drain conductance, g_d (= $\partial I_D/\partial V_D$), can be generally expressed, based on (3.6), (3.10), and (3.15), as

$$g_d = \frac{Z}{L} \mu_{nf} C_{of} \left[V_{Gf} - V_{Tf} - (1 + \frac{C_{body}}{C_{of}}) V_D\right] \tag{3.18}$$

where V_{Tf} is given by (2.8) or (2.12) depending on V_{Gb}, and where the effective body capacitance C_{body} varies from C_b to C_{bb} as the back-surface charge condition is changed from accumulation to depletion. In contrast to the bulk MOSFET, C_{body} is a constant independent of V_D when

the back-surface charge condition is uniform. Thus g_d decreases linearly with increasing V_D and the slope is determined by V_{Gb}, which defines C_{body}. We plot in Fig. 3.3 measured and calculated $g_d(V_D)$ for V_{Gf} = 4 V and 6 V and for V_{Gb} = 0 V and -80 V. We have good agreement between theory and experiment except for V_{Gf} = 6 V and V_D < 1 V where the measured g_d is considerably lower due to the mobility degradation. The influence of V_{Gb} on the slope of the plots is apparent from the data. Note that for $V_{Gb} < V_{Gb}^A$, $C_{body} = C_b$ when V_D is low enough that $V_{Gb} < V_{Gb}^A(L)$; otherwise, for higher V_D, $C_{body} = C_{bb}$. Hence for such intermediate-V_{Gb} cases, the $g_d(V_D)$ characteristic will show a change of slope at the value of V_D defined by $V_{Gb}^A(L) = V_{Gb}$.

Measured dependences of $I_{D(sat)}$ on V_{Gf} ($=V_D$) are plotted with the calculated dependences in Fig. 3.4 for V_{Gb} = 0 V, -20 V, and -80 V. We have good agreement between theory and experiment except for the high-V_{Gf} portion of the V_{Gb} = -80 V curve, where the mobility degradation again reduces the current considerably. The theory, based on constant μ_{nf}, predicts about a 30% decrease in $I_{D(sat)}$ at V_{Gf} = 8 V when V_{Gb} decreases from 0 V to -80V. Actually, because of the mobility degradation, the measured current decreases by 35%. The V_{Gb} = -20 V curve is plotted to show the $I_{D(sat)}(V_{Gf})$ characteristic for a nonuniform back-surface charge condition. The plot coincides with the V_{Gb} = -80 V curve at low V_{Gf} until the back surface becomes depleted near the drain at $V_{Gf} \approx 3$ V. For larger V_{Gf} values, the drain current was calculated from $I_{D(sat)}^{AD}$ in (3.15) where $V_{Gb}^A \approx -6$ V was determined from the $I_{D(sat)}(V_{Gb})$ measurement using

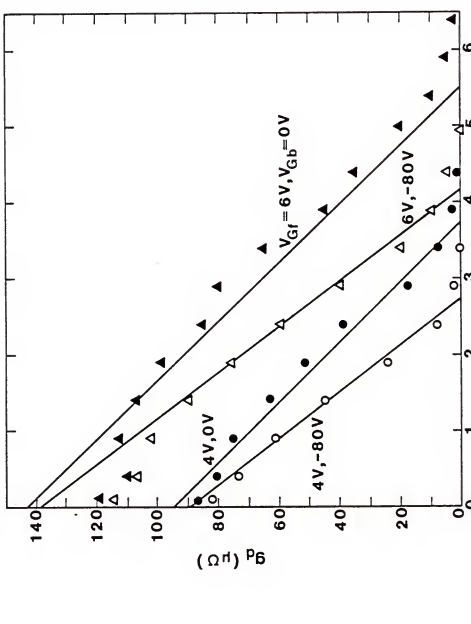

Figure 3.3 Measured (points) and calculated (lines) drain conductance versus the terminal voltages of the SOI MOSFET. The discrepancies between the theoretical and experimental results at low V_D are due to mobility degradation.

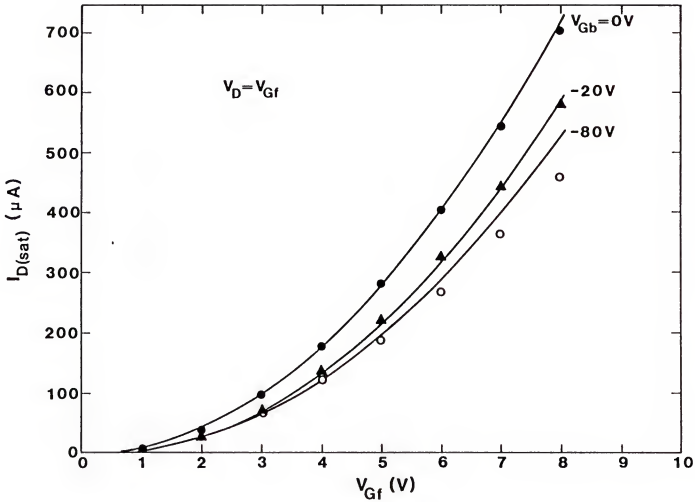

Figure 3.4 Measured (points) and calculated (curves) saturated drain current versus the gate voltages of the SOI MOSFET. The measurements were made with the drain terminal connected to the front gate. The discrepancy for high V_{Gf} and V_{Gb} = -80 V is due to mobility degradation.

$$\left.\frac{I_{D(sat)}}{I^{A}_{D(sat)}}\right|_{V_{Gb}=V^{A}_{Gb}} = \frac{1 + C_b/C_{of}}{1 + C_{bb}/C_{of}} \quad . \tag{3.19}$$

The relationship (3.19), which follows from (3.9) and (3.12), provides a theoretical basis for determining V^{A}_{Gb} from $I_{D(sat)}(V_{Gb})$ measured at low V_{Gf} such that μ_{nf} has negligible dependence on V_{Gb}. The use of (3.19) is exemplary of the utility of our simplified model.

The dependence of $I_{D(sat)}$ on V_{Gb} is illustrated in more detail in Fig. 3.5. For a given value of V_{Gf}, we see that $I_{D(sat)}$ decreases with decreasing V_{Gb} until it saturates when the back surface becomes completely accumulated [at $V_{Gb} = V^{A}_{Gb}(L)$]. Note that $V^{A}_{Gb}(L)$ decreases (becomes more negative) with increasing V_{Gf} as predicted by (3.5) and (3.8). The slight discrepancies between the measured and calculated $I_{D(sat)}$ at low V_{Gb} and high V_{Gf} are due to the mobility degradation discussed previously. The discrepancies in $V^{A}_{Gb}(L)$ are probably due to surface states at the back $Si\text{-}SiO_2$ interface, which tend to stretch-out the curves as shown in Chapter Two.

The dependence of $V_{D(sat)}$ on V_{Gf} and V_{Gb} is shown in Fig. 3.6. As predicted by (3.8) and (3.11), $V_{D(sat)}$ increases linearly with increasing V_{Gf} unlike the bulk MOSFET characteristic, and the slope is again determined by V_{Gb}. Two methods were used to measure $V_{D(sat)}$ to better support the analysis. First, from the $g_d(V_D)$ plots in Fig. 3.3, $V_{D(sat)}$ was taken as the intercept of the linear extrapolation on the V_D axis. Second, $V_{D(sat)}$ was taken as the value of V_D at which I_D is 99%

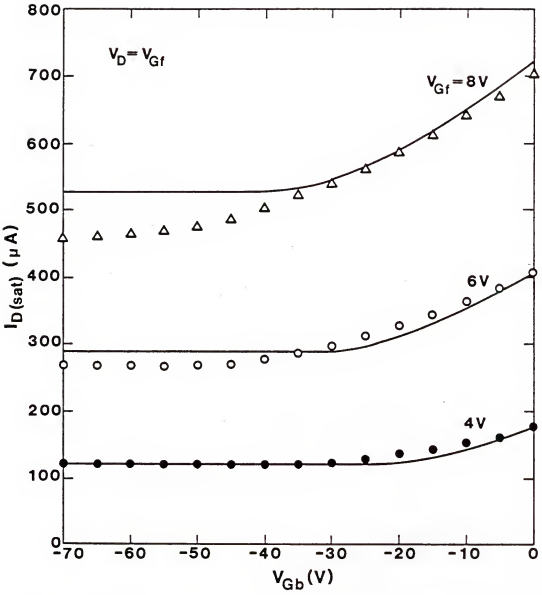

Figure 3.5 Measured (points) and calculated (curves) dependences of $I_{D(sat)}$ on V_{Gb}.

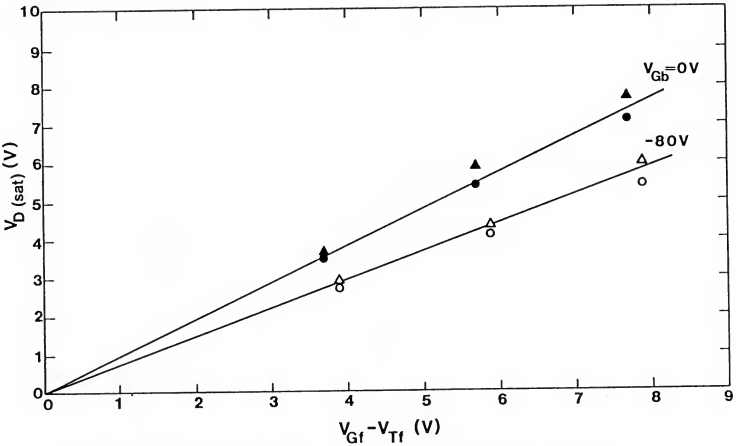

Figure 3.6 Measured (points) and calculated (lines) drain saturation voltage versus the gate voltages of the SOI MOSFET. The triangular data points were estimated from the $g_d(V_D)$ plots in Fig. 3.3; the circular data points were obtained by taking the value of V_D at which I_D is 99% of $I_{D(sat)}$ in Fig. 3.4. Note that V_{Tf} is 0.1 V and 0.3 V for V_{Gb} equal to 0 V and -80 V respectively.

of $I_{D(sat)}$ in Fig. 3.4. Both measured values agree well with the theoretical predictions; the influence of V_{Gb} is modeled well.

The SOI MOSFET transconductance, g_m $(=\partial I_D/\partial V_{Gf})$, differs considerably from that of the bulk counterpart in the saturation region. From (3.9), (3.12), and (3.17),

$$g_{m(sat)} = \frac{Z}{L} \frac{\mu_{nf} C_{of}}{(1 + C_{body}/C_{of})} (V_{Gf} - V_{Tf}) \tag{3.20}$$

varies linearly with V_{Gf}, unlike in the bulk MOSFET, and depends on V_{Gb} through V_{Tf} and C_{body} defined previously with reference to (3.18). For high V_{Gf}, the device comes out of saturation, and from (3.6), (3.10), and (3.15),

$$g_m = \frac{Z}{L} \mu_{nf} C_{of} V_D \tag{3.21}$$

like in the bulk MOSFET. Calculated and measured values of $g_m(V_{Gf})$ at V_D = 4 V for V_{Gb} = 0 V and -80 V are plotted in Fig. 3.7. For low V_{Gf}, (3.20) applies and the influence of V_{Gb} on the slope of the characteristic is evident. For high V_{Gf}, g_m is independent of V_{Gb} as predictd by (3.21). The measured g_m in this region is 20-25% lower than the predicted g_m, which is consistent with the previously estimated mobility degradation. The plots support our notion that the μ_{sat} degradation due to high V_{Gf} is much more severe when the back surface is accumulated (V_{Gf} = 3-5V) and that the μ_{lin} degradation is almost independent of V_{Gb} (V_{Gf} = 6-8 V).

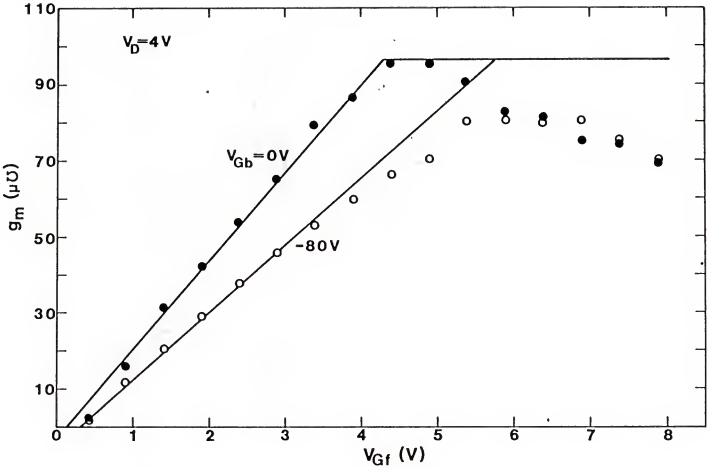

Figure 3.7 Measured (points) and calculated (lines) transconductance at V_D = 4 V versus the gate voltages of the SOI MOSFET. The discrepancies for high V_{Gf} are due to mobility degradation.

As intimated by our theoretical-experimental analysis, the drain current of an SOI MOSFET can be either higher or lower than that of the bulk counterpart depending on V_{Gb}. Typically the conductance of the SOI MOSFET is higher than that of the bulk MOSFET when the back surface is depleted, and lower when the back surface is accumulated. The optimal V_{Gb} bias, at which I_D is maximized without increased leakage current, is theoretically V_{Gb}^A (when $t_b < x_{d(max)}$). At this bias, when the device is ON, I_D is high because the body capacitance (C_{bb}) is small, and when the device is OFF, the leakage current is minimized. Increasing V_{Gb} above V_{Gb}^A might increase the OFF leakage whereas lowering V_{Gb} reduces the ON current.

Reducing the silicon film body thickness, which is necessary for fine lithography, results in strong charge-coupling and hence more significant influence of V_{Gb} on the (front-channel) current-voltage characteristics. This influence can be used advantageously for some applications. For example, an SOI MOSFET in a low-doped silicon film, in which the carrier mobility is high, can have an acceptable threshold voltage if V_{Gb} is properly selected.

From our analysis we see that the dependence of I_D on V_{Gb} is described by an effective silicon film body capacitance C_{body}, which decreases from C_b to C_{bb} as V_{Gb} alters the back-surface charge condition from accumulation to depletion. This capacitance, which is determined by the thicknesses of the silicon film and the back insulator, is independent of N_A as long as the film is completely depleted. Thus, except for the threshold voltage, the current-voltage characteristics of

a completely depleted SOI MOSFET are virtually insensitive to the actual doping density profile $N_A(x)$.

When the deep boron implant is done to suppress the back surface leakage current of n-channel device, as described in Subsection 2.3.2, the highly doped region near the back surface is not depleted when V_D is low. Since the highly doped region at the back surface is tantamount to an accumulation layer, I_D is given by I_D^A in (3.6) with t_s replacing t_b. At high V_D (~5 V typically) however, even this highly doped region can be depleted near the drain, rendering the front channel conductance dependent on V_{Gb}: thus I_D for this case can be modeled similarly to I_D^{AD}. Heavy deep boron implantation will suppress I_D because, in addition to increasing V_{Tf}, it tends to prevent depletion at the back surface and hence results in higher body capacitance.

3.4 Summary

Simple closed-form expressions for the steady-state drain current of SOI MOSFET in the strong inversion have been derived using the one-dimensional charge-coupling analysis in Chapter Two. The model was simplified, without significant loss of accuracy, by recognizing that Q_n is approximated well by a linear function of the surface potential, which describes Q_n exactly when the silicon film is completely depleted. The I_D expressions, which are simpler than those for bulk MOSFETs when the back surface charge condition is uniform, clearly show the dependence of the current-voltage characteristics on the back-gate bias V_{Gb} and on the device parameters, e.g., the silicon film thickness and the doping density.

The analysis was supported by measurements of current-voltage characteristics of thin-film SOI MOSFETs fabricated in laser-recrystallized silicon. These measurements included the dependences of drain current (I_D, $I_{D(sat)}$), of conductances (g_d, g_m), and of saturation voltage ($V_{D(sat)}$) on the terminal voltages (V_{Gf}, V_{Gb}, V_D), and agreed well with the theoretical predictions. Some discrepancies were noted, but were attributed to the degradation of carrier mobility at high V_{Gf}, especially for low V_D and/or when the back surface is accumulated. The average mobility in the saturated device (μ_{sat}) has a strong dependence on V_{Gb}, which enhances the influence of V_{Gb} on I_D.

The drain current of the thin-film SOI MOSFET can be either higher or lower than that of the bulk MOSFET, for a given threshold voltage and mobility, depending on the back-surface charge condition as determined by V_{Gb} and the back $Si\text{-}SiO_2$ properties. We note that the high (saturated) current drive capability of the SOI MOSFET relative to the bulk counterpart that has been reported [51] and attributed to high carrier mobility is quite possibly due to the low effective body capacitance (C_{bb}) that obtains when the back surface is depleted. With the leakage current minimized, the drain current will be maximized when V_{Gb} is biased at V_{Gb}^{A}, i.e., at the onset of back-surface accumulation at the source. At this bias, the back surface is depleted when the device is ON, whereas when the device is OFF the back surface is accumulated and the leakage current is suppressed.

CHAPTER FOUR
FLOATING-BODY EFFECTS IN TRANSIENT CONDITIONS

4.1 Introduction

An important feature of the common four-terminal SOI MOSFET is its floating body, a familiar consequence of which is the "kink" in the steady-state $I_D(V_D)$ characteristic [24,27]. The kink occurs in the saturation region when (in the n-channel transistor) majority holes are generated by impact ionization at the drain and are swept into the floating body. The resulting excess holes in the body raise its quasi-neutral region potential V_B (i.e., the source-body forward bias), and thereby lower V_{Tf} [24,27].

A more important effect of the floating body is the transient overshoot in drain current that occurs when the device is turned ON [29]. This overshoot results because excess holes, generated during the OFF state, cannot be removed from the floating body instantaneously. Instead they raise V_B like in the kink effect and produce an excessive transient channel current. The transient I_D decays to the steady-state value as the excess holes are removed through recombination processes at the forward-biased source-body junction. Since the propagation delay τ_{pd} of an MOS digital circuit stage is determined mainly by the magnitude of the initial drain current available to (dis)charge the load

capacitance [29], the overshoot in I_D can significantly affect the speed of SOI MOS circuits.

Eaton and Lalevic [28,29] studied transient effects due to the floating body of SOS MOSFETs. They experimentally demonstrated dependences of the transient I_D and τ_{pd} on the switching frequency, and theoretically explained them by describing a time-dependence for the threshold voltage in the linear region. A more quantitative treatment of the frequency dependence must describe the transient drain saturation current $I_{D(sat)}$, which is directly related to τ_{pd} [35]. Also for the SOI MOSFET, the strong dependence of the transient $I_{D(sat)}$ on V_{Gb} must be accounted for.

In this chapter we analyze the transient effects of the floating body in thin-film enhancement-mode SOI MOSFETs, accounting for the charge coupling. The analysis quantitatively describes the frequency-dependent transient $I_{D(sat)}$ for various back-surface charge conditions, which in turn is related to τ_{pd} of an SOI CMOS inverter. The transient $I_{D(sat)}$ is modeled by combining a quasi-static characterization of $I_{D(sat)}(V_B)$, which is derived by generalizing the current-voltage analysis in Chapter Three, with a description of the time-dependent $V_B(t)$, which is based on models for carrier generation in the OFF state and carrier recombination in the ON state.

To simplify the analysis, a step function is assumed for the front-gate turn-ON pulse, but the effects of a finite rise time are discussed. The analysis reveals that typically the magnitude of the overshoot in I_D is not sensitive to the rise time because $V_B(t)$ decays

slowly. We also assume a uniform doping density in the film body, but extension of the analysis to account for nonuniform doping densities is discussed.

Measurements of transient $I_{D(sat)}$ in thin-film MOSFETs fabricated in (graphite-strip-heater) recrystallized SOI were made and are shown to support the analysis. The measured currents clearly show predicted dependences on switching frequency and on V_{Gb}. Measurements of τ_{pd} of CMOS inverters were made using cascades of inverters and ring oscillators fabricated on the same SOI test chip. The observed dependences of τ_{pd} on frequency and V_{Gb} are explained by our analysis and the simple inverse relationship between τ_{pd} and $I_{D(sat)}$ developed by Burns [35]. The measurements show that the peak value of the transient $I_{D(sat)}$, rather than the steady-state value, defines the frequency-dependent τ_{pd}.

4.2 Transient Drain Current

We first derive the drain current expression for arbitrary V_B and then characterize the time-dependent $V_B(t)$ by modeling the carrier generation/recombination in the OFF/ON states.

4.2.1 Dependence of I_D on V_B and V_{Gb}

Although V_B is time-dependent in dynamic operation, the quasi-static $I_D(V_B)$ model will describe the time-dependent $I_D(t)$ adequately since the redistribution speed [52,53] of inversion charge is typically much faster than the variation rate of $V_B(t)$.

The general characterization of the quasi-static I_D is complicated since the film body might not be completely depleted for all possible ON conditions. In this case, the $Q_{nf}(\psi_{sf})$ relationship is nonlinear. We showed however in Appendix B that the expression for I_D is simplified with good accuracy by using the linear $Q_{nf}(\psi_{sf})$ relationship (3.3) even when the film body is incompletely depleted. Since this simplification is basically a linearization of the body depletion capacitance, the error implied by it is determined by the body capacitance relative to C_{of}. Although the error increases with increasing V_B, it is not significant (< 10%) for a typical, saturated SOI MOSFET with a thin gate oxide ($t_{of} \sim 500$ A), and hence (3.3) is a useful approximation for most operating conditions.

When the back surface is accumulated, evaluation of (3.2) using (3.3) with $\psi_{sb}(y) \simeq V_B$ yields

$$I_D = I_D^a = \frac{Z}{L} \mu_{nf} C_{of} \left[(V_{Gf} - V_{Tf}^a) V_D - \left(1 + \frac{C_b}{C_{of}}\right) \frac{V_D^2}{2} \right] \tag{4.1}$$

where

$$V_{Tf}^a = V_{FB}^f + \left(1 + \frac{C_b}{C_{of}}\right) 2\Phi_B - \frac{Q_b}{2C_{of}} - \frac{C_b}{C_{of}} V_B \quad . \tag{4.2}$$

The saturation current is

$$I_{D(sat)} = I^{a}_{D(sat)} = \frac{Z}{L}\mu_{nf}C_{of}\frac{(V_{Gf} - V^{a}_{Tf})^2}{2(1 + C_b/C_{of})}$$

$$= I^{A}_{D(sat)}\left[1 + \frac{C_b V_B}{C_{of}(V_{Gf} - V^{A}_{Tf})}\right]^2 \qquad (4.3)$$

where $I^{A}_{D(sat)}$ and V^{A}_{Tf} are $I^{a}_{D(sat)}$ and V^{a}_{Tf} in the steady state ($V_B = 0$) as defined previously. Hence the significance of the overshoot current $[I^{a}_{D(sat)} - I^{A}_{D(sat)}]$ is determined by C_b/C_{of} and $V_B/(V_{Gf} - V^{A}_{Tf})$.

When the back surface is depleted or inverted, the effects of the floating body will be less significant. In these cases, fewer excess holes are stored in the body during the OFF state because the back gate depletes a portion of the body, independent of V_{Gf}. Therefore the transient overshoot in I_D is smaller, and in fact for V_{Gb} high enough to deplete most of the film body, the steady-state $I_D(V_D, V_{Gf}, V_{Gb})$ model in Chapter Three can be used for dynamic operation also.

4.2.2 Time Dependence of V_B

To characterize the transient $I_{D(sat)}(t)$, which often controls the speed of SOI circuits, we must incorporate the time dependence of V_B in the ON state into (4.3). After abrupt turn-on, the initial value of $V_B(t)$ is defined by the number of excess holes generated and stored in the film body during the preceding OFF state. The decay of $V_B(t)$ is governed by the rate of hole removal through recombination during the ON state.

When the device is turned OFF abruptly, V_B is negative due to the intact depletion charge in the body. The potential then increases

toward zero in time as the depletion region shrinks due to hole-electron-pair generation. Since the electric field in the depletion region is directed toward the back surface, the generated holes neutralize the depletion charge starting at the back surface, while the generated electrons are swept to the front surface and out the drain. The generated holes are stored in the film body until the depletion-region width reaches its steady-OFF-state value, x_{do}, at which $V_B = 0$. (We implicitly assume $x_{do} > 0$, which precludes front-surface accumulation in the steady OFF state.) Beyond this point, the generated holes contribute to the drain-source leakage current.

Assuming a uniform carrier generation rate G in the depletion region (surface generation is negligible) and neglecting the small variation in the back-surface accumulation charge ($\Delta Q_{cb} \simeq C_{ob}\Delta V_B$ in the OFF state), we can express the rate of increase in the number (N_h) of excess (referenced to the steady ON state) holes in the body as

$$\frac{dN_h}{dt} \simeq GZL\left(x_{di} - \frac{N_h}{ZLN_A}\right) \tag{4.4}$$

where x_{di} is the initial depletion-region width when the device is turned OFF from the steady ON state. Because most of the film body is depleted when the device is ON (saturated), $x_{di} \simeq t_b$. The few holes in the body redistribute via dielectric relaxation, vis-a-vis, virtually instantaneously, to make x_{di} constant along the channel.

Based on Shockley-Read-Hall theory [54], we assume $G \approx n_i/\tau_g$ where τ_g is the sum of the hole and electron effective emission times. Then the solution of (4.4), with $x_{di} \approx t_b$, is

$$N_h(t_{off}) \approx ZLt_bN_A \left[1 - \exp(-\frac{t_{off}}{\tau_G})\right] \tag{4.5}$$

where

$$\tau_G \equiv \frac{N_A}{n_i} \tau_g \tag{4.6}$$

is much longer than τ_g. The solution (4.5) is valid for OFF-time $t_{off} < t_o$ where t_o is the time at which the device reaches the steady OFF state ($x_d = x_{do}$, $V_B = 0$). For $t_{off} > t_o$,

$$N_h \approx ZL(t_b - x_{do})N_A \quad ; \tag{4.7}$$

it does not increase further as the generated holes now recombine in the quasi-neutral body region, contributing to source-drain leakage current. Equating (4.5) and (4.7) defines

$$t_o \approx \tau_G \ln(\frac{t_b}{x_{do}}) \quad . \tag{4.8}$$

The steady-OFF-state depletion-region width x_{do} is easily related to V_{Gf} using conventional MOS theory [32]:

$$V_{Gf(OFF)} = V_{FB}^{f} + \frac{qN_A X_{do}^2}{2\varepsilon_s} + \frac{qN_A X_{do}}{C_{of}} \quad , \tag{4.9}$$

which when rewritten for X_{do}, yields

$$X_{do} = \frac{\varepsilon_s}{C_{of}} \{[1 + \frac{2C_{of}^2(V_{Gf(OFF)} - V_{FB}^{f})}{qN_A\varepsilon_s}]^{1/2} - 1\} \quad . \tag{4.10}$$

When the device is turned ON by a step pulse at the front gate, inversion charge is injected into the channel from the source very quickly as defined by the electron transit time [52,53]. Concurrently the $\psi_{sf}(y)$ gradient, defined by V_D, is established and forces the holes in the film body toward the source. These holes cannot be removed freely from the floating body, and hence they produce a forward bias V_B on the source-body junction, which quickly injects electrons into the body to neutralize the region containing the excess holes. After these fast transients, which occur in negligibly short time, V_B begins to decay as the excess holes are removed through recombination processes associated with the forward-biased source-body junction.

The initial value of V_B is defined by N_h, given by (4.5) or (4.7), from the condition of quasi-neutrality in the body where the excess holes are stored. With reference to Fig. 4.1, the excess holes must neutralize the acceptor ions in the excess (referenced to the steady ON-state) quasi-neutral region as well as the injected electrons, and must supply ΔQ_{cb}:

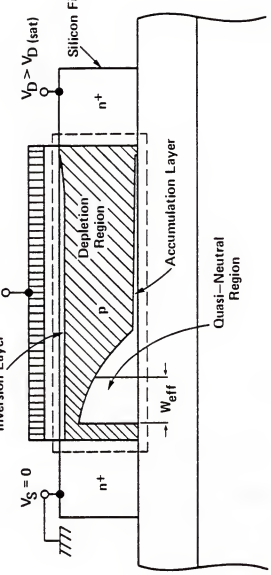

Figure 4.1 Illustration of charge distribution in the film body of a saturated SOI MOSFET with accumulated back surface. The dashed lines indicate the surface around which Gauss's theorem is applied to evaluate charge components in (4.11).

$$N_h = N_A \Delta V + \int_V \Delta n dV + \frac{1}{q} ZL\ \Delta Q_{cb} \tag{4.11}$$

where Δn is the excess electron density, and ΔV and V are the volumes of the excess and total neutral regions. The first and last components of N_h in (4.11) define actual changes (with respect to the steady ON state) in net charge and hence can be evaluated by applying Gauss's theorem around the floating body as indicated in Fig. 4.1:

$$qN_A \Delta V + ZL\ \Delta Q_{cb} + Z \int_0^L \Delta Q_{nf} dy = Z \int_0^L (C_{of} \Delta \psi_{sf} + C_{ob} \Delta \psi_{sb}) dy \tag{4.12}$$

where ΔQ_{nf} is the change in the inversion charge density from the steady ON state, and the integrand on the right side comprises the changes in the normal electric flux density in the front and back oxides.

We now evaluate the integrals in (4.12). For the assumed condition of back-surface accumulation, $\Delta \psi_{sb} = V_B$, independent of y. We show in Appendix D that in the saturation region, $\Delta Q_{nf}(y) \approx \Delta Q_{nf}(0)[1-y/L]^{1/2}$ and $\Delta \psi_{sf}(y) \approx \Delta V_{D(sat)}(1 - [1 - y/L]^{1/2})$ where $\Delta V_{D(sat)}$ is the change in the drain saturation voltage from the steady ON state. We stress that, in contrast to the bulk MOSFET, these approximations are generally valid because of the nearly constant body capacitance along the channel. From the $Q_n(\psi_{sf})$ in (3.3), with V_{Gf} fixed at its steady-ON-state value and $\Delta \psi_{sb} = V_B$, we get $\Delta Q_{nf}(0) = -C_b V_B$ and $\Delta V_{D(sat)} = \Delta \psi_{sf}(L) = [C_b/(C_b + C_{of})]V_B$. Thus (4.12) yields

$$N_A \Delta V + \frac{1}{q} ZL\ \Delta Q_{cb} = \frac{ZLC_{eff}}{q} V_B \tag{4.13}$$

where

$$C_{eff} \triangleq C_b + C_{ob} - \frac{C_b}{3(1 + \frac{C_{of}}{C_b})} \quad , \tag{4.14}$$

which typically is approximately C_b.

The integral in (4.11) which reflects electron injection from the source and the channel near the source, can be approximated by treating the quasi-neutral region illustrated in Fig. 4.1 as being one-dimensional (in the y-direction) and having an effective width W_{eff} that is shorter than the electron diffusion length. Then from short-base diode theory [32],

$$\begin{aligned} \int_V \Delta n dV &\simeq \frac{Zt_b W_{eff}}{2} \frac{n_i^2}{N_A} \exp(\frac{qV_B}{kT}) \\ &\equiv \frac{Zt_b W_{eff}}{2} N_A \exp[\frac{q(V_B - 2\phi_B)}{kT}] \quad . \end{aligned} \tag{4.15}$$

Although W_{eff} depends on V_B and V_{Gf}, as can be shown by accounting for the actual geometry of the quasi-neutral region, these dependences are negligible compared to the exponential dependence in (4.15). In fact we now show that the relationship between V_B and N_h can be approximated knowing only that $W_{eff} \leq L$.

This relationship is defined by inserting (4.13) and (4.15) into (4.11). Noting that (4.13) is linear in V_B and (4.15) is exponential in V_B, and that they are comparable in magnitude when $V_B \simeq 2\phi_B$, we can simplify the relationship as follows:

$$V_B \simeq \frac{q}{ZLC_{eff}} N_h \qquad \text{for} \qquad N_h < \frac{ZLC_{eff}}{q} (2\phi_B) \tag{4.16}$$

and

$$V_B \simeq 2\phi_B \qquad \text{for} \qquad N_h > \frac{ZLC_{eff}}{q} (2\phi_B) \quad . \tag{4.17}$$

This result is generally applicable when the device is ON (in the saturation region). The peak value of V_B, V_{BP}, which obtains immediately after turn-ON, is defined by using (4.5) or (4.7) in (4.16) and (4.17). Actually N_h is reduced during the turn-ON due to fast hole injection into the source and to recombination in the body during the finite rise time of the gate pulse. However, this change has a negligible effect on V_B because for high N_h, V_B is independent of N_h and for low N_h, the change is small compared to N_h.

After the device is turned ON (at $t_{on} = 0$), V_B decays in time as N_h is reduced by the recombination processes associated with the forward-biased source-body junction. These processes occur in the quasi-neutral source and junction space-charge regions as well as in the quasi-neutral body region. For high N_h, where (4.17) applies, the recombination in the quasi-neutral regions is predominant [32]; but V_B does not change appreciably in time. For N_h low enough that (4.16) applies, i.e., for $V_B < 2\phi_B$ by a few thermal voltages, the recombination in the junction space-charge region is predominant. The rate of this recombination can be approximated as [32]

$$-\frac{dN_h}{dt} \approx \frac{Zt_b W_{SCR}}{\tau_r} N_A \exp\left[\frac{q(V_B - 2\phi_B)}{2kT}\right] \tag{4.18}$$

where W_{SCR} is the effective width of the space-charge region and τ_r is the effective carrier recombination lifetime in the region. Comparison of (4.18) with (4.15), which when divided by the electron lifetime gives the recombination rate in the quasi-neutral body region, confirms the stated predominance of the space-charge region recombination.

Combining (4.16) and (4.18), we obtain a differential equation in time that can be solved to yield

$$V_B(t_{on}) \approx V_{BP} - \frac{2kT}{q} \ln\left\{1 + \frac{q^2 t_b W_{SCR} N_A}{2kTC_{eff}L} \exp\left[\frac{q(V_{BP} - 2\phi_B)}{2kT}\right]\left(\frac{t_{on}}{\tau_r}\right)\right\} . \tag{4.19}$$

Although this logarithmic decay of V_B is strictly valid when V_B is a few thermal voltages below $2\phi_B$, it can be used generally even when $V_{BP} \approx 2\phi_B$, corresponding to (4.17), because the time required for V_B to drop by a few thermal voltages is negligibly short. Consequently the transient saturation current is described completely by the combination of (4.3) and (4.19).

From (4.19), we note that the maximum decay rate of $V_B(t_{on})$ is $\sim kT/q\tau_r$. Since the propagation delay (τ_{pd}) of an SOI MOS digital circuit stage is typically shorter than τ_r (see Sec. 4.3), the decay in V_B during the delay is negligibly small. Therefore, for the assumed abrupt turn-ON,

$$V_B \simeq V_{BP} \tag{4.20}$$

during the delay, and hence the peak $I_{D(sat)}$ in (4.3) can be used to estimate τ_{pd} [35].

We illustrate in Fig. 4.2 the time-dependences of N_h, V_B, and $I_{D(sat)}$ over a period of the gate voltage when the device is switching at such a low frequency that it reaches steady state during each half-cycle. Shapes and magnitudes of the plots are defined by the equations shown in the figure.

4.3 Experimental Results and Discussion

To provide experimental support for the analysis in Section 4.2, we measured the transient $I_{D(sat)}$ and τ_{pd}, at various operating frequencies and back-gate biases, of four-terminal SOI MOSFETs and CMOS inverters, respectively. The devices were fabricated at Texas Instruments, Inc. [33] in 0.4-μm-thick SOI films that were recrystallized using a graphite-strip heater after being deposited on an 8000-Å-thick SiO_2 layer, which had been thermally grown on a silicon substrate (p-type, 6-8 Ω-cm). The front gate is n^+ polysilicon and the gate oxide is 500-Å-thick.

4.3.1 Transient Drain Current

Discrete n-channel MOSFETs were used to measure $I_{D(sat)}(t)$. The devices are relatively large (Z = 300 μm, L = 7.5 μm) with closed

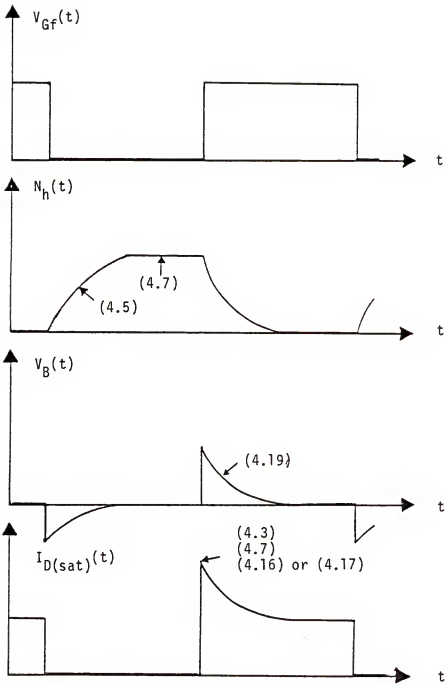

Figure 4.2 Illustration of the time-dependences of N_h, V_B, and $I_{D(sat)}$ over a period of a low-frequency gate voltage. Equation numbers describing the magnitude and shape of the plots are given.

geometry. The film body was doped by shallow and deep boron implants that yielded $N_A \approx 1.5 \times 10^{16}$ cm^{-3} near the front surface and $N_A \approx 6 \times 10^{16}$ cm^{-3} at the back surface [33]. Although N_A is not uniform, our analysis, which is based on a constant-N_A assumption, is applicable if t_b is modified properly. The highly doped region of the film body, when not depleted, is tantamount to an accumulation layer at the back surface as shown in Subsection 2.3.2, and hence replacing t_b with the thickness t_s of the lowly doped region of the film body renders the analysis applicable. It is interesting to note that the deep boron implant, which defines the thinner effective film thickness (t_s), enhances the transient overshoot in $I_{D(sat)}$, as shown by (4.3), and widens the range of V_{Gb} for which the overshoot is significant and the analysis applies.

The circuit configuration used for the measurement is shown in Fig. 4.3. The time-dependent current was obtained by measuring the voltage drop across the load resistor. A small resistance (R_L = 1 KΩ) was used to keep the MOSFET in the saturation region and to reduce the (dis)charging time of the probe input capacitance (C_p). A low supply voltage (V_{DD} = 1.5V) was selected because the frequency dependence of $I_{D(sat)}(t)$ is more pronounced at low V_{DD} as indicated in (4.3) with $V_{Gf} = V_{DD}$. The rise time (t_r) of the input pulse is ≈ 30 ns.

We plot in Fig. 4.3 the measured peak $I_{D(sat)}$, i.e., $I_{D(sat)}(t_{on} \approx 0)$, versus switching frequency f_s for V_{Gb} ranging from -10 V to +10 V. Also plotted in the figure is the peak $I_{D(sat)}$

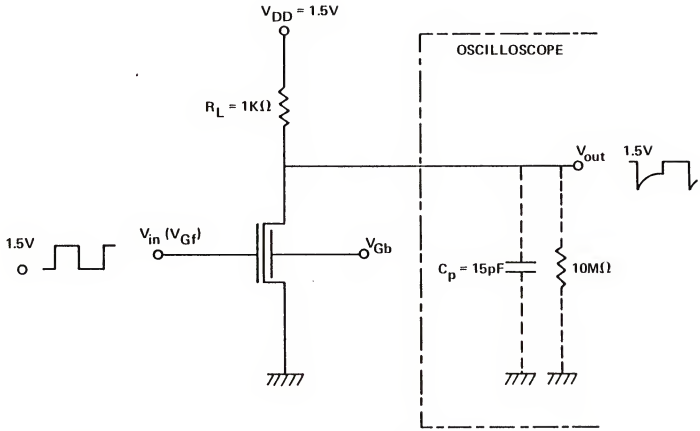

Figure 4.3 Circuit configuraton used to measure the frequency dependence of the transient $I_{D(sat)}$ for various values of V_{Gb}.

calculated using (4.3), in which $t_b + t_s \simeq 0.3$ μm, $I^A_{D(sat)} = 55$ μA and $V^A_{Tf} = 1.1$ V were measured in the steady ON state, and $V_B = V_{BP}$ is evaluated from (4.5), (4.7), (4.16), and (4.17). We use (4.5), in which $t_{off} = 1/2f_s$, irrespective of the fact that for high f_s the steady ON state never obtains. The consequent error in (4.5) is unimportant because $I_{D(sat)}$ at high f_s is close to the steady-ON-state value as shown in Fig. 4.4. We note that the calculated peak-$I_{D(sat)}$ curve agrees well with the measured ones provided $V_{Gb} \leq -5$ V for which the back surface is (effectively) accumulated. At low f_s, the peak $I_{D(sat)}$ is maximum corresponding to (4.16), independent of f_s; whereas at high f_s, it is minimum, near but higher than the steady-ON-state value. This minimum corresponds to a virtually fixed $N_h \geq 0$ defined by the equality of (4.4) and (4.18), which are nearly constant at high f_s. The theoretical-experimental correlation implies $\tau_g \simeq 40$ nsec. (Since $\tau_r \sim \tau_g > t_r$, our neglect of the effect of a finite rise time on V_{BP} and the peak $I_{D(sat)}$ is justified.)

Based on our analysis, we can explain qualitatively the dependence on V_{Gb} illustrated in Fig. 4.4. The overshoot in $I_{D(sat)}$, which is the difference between the peak $I_{D(sat)}$ and the steady-ON-state value, is approximately the difference between the low- and high-f_s values of the peak $I_{D(sat)}$ for each V_{Gb} value plotted in Fig. 4.4. We see that it decreases as V_{Gb} increases in accordance with the discussion in Section 4.2 concerning the case for which the back surface is depleted or inverted. It does not decrease appreciably however until $V_{Gb} > 0$ even though the back surface is strongly inverted and conducting as evidenced

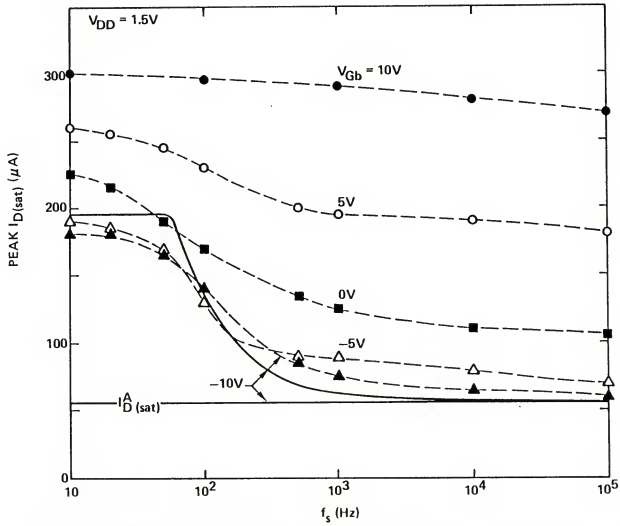

Figure 4.4 Measured (points) and calculated (solid line) dependences on f_s of the peak $I_{D(sat)}$ for V_{Gb} = -10V to 10V. The steady-state value $I^{A}_{D(sat)}$, measured at V_{Gb} = -10V, is shown for reference. The calculated V_{BP} varies from $2\phi_B$ at low f_s ($< \approx$ 70 Hz) to near zero at high f_s ($> \sim$ 1 KHz).

by the increased steady-ON-state (high-f_s) current. This sustained overshoot is due to the highly doped region in the film body near the back surface produced by the deep boron implant. This region is not completely depleted for $V_{Gb} < 0$, and hence the transient effects in the floating body remain significant. Only when V_{Gb} is sufficiently high (~ 10 V) to deplete the entire highly doped region near the drain will the overshoot be suppressed. The high value of V_{Gb} is necessary to induce a sufficiently high ψ_{sb} ($\simeq 2\phi_B + V_{DD}$) at the pinch-off point in the back channel because of the thick (8000 Å) back oxide.

4.3.2 Propagation Delay

To investigate the influence of the transient drain current on circuit speed, we measured the dependences on f_s and V_{Gb} of propagation delay in SOI CMOS test circuits. The dependence on f_s was measured using a cascade of nine inverters, and the dependence on V_{Gb} was measured using a 39-stage ring oscillator.

The CMOS inverter comprises an n-channel SOI MOSFET (driver), which is identical to the discrete device described previously but is smaller (Z_n = 30 μm, L_n = 5 μm), and a p-channel SOI MOSFET (load), which has a threshold voltage near zero (Z_p = 45 μm, L_p = 5 μm). The film body of the p-channel device was doped by ion implantation such that it is p-type ($N_A \simeq 10^{16}$ cm^{-3}) near the front surface and n-type ($N_D \simeq 4 \times 10^{15}$ cm^{-3}) near the back surface [33]. The physical structure of both MOSFETs, i.e., the SOI film and the oxides, is the same.

Burns [35] showed using computer simulation that the propagation delay of a single stage in a long cascade of CMOS inverters can be empirically related to the saturation currents (at $|V_{Gf}| = V_{DD}$) of the n- and p-channel devices by

$$\tau_{pd} \simeq 0.9\, C_L V_{DD} \left[\frac{1}{I^n_{D(sat)}} + \frac{1}{I^p_{D(sat)}}\right] \tag{4.21}$$

where C_L is the load capacitance, assumed to be constant. Although (4.21) was derived neglecting the effects of finite carrier transit time in the channel, Swanson [55] showed that the effects are typically insignificant. To apply (4.21) to SOI CMOS, we use the peak value of the transient $I_{D(sat)}$, as suggested by our analysis, and we let $C_L = C_{of}(Z_n L_n + Z_p L_p)$, which although crude nonetheless facilitates a semi-quantitative description of the effects of the transient $I_{D(sat)}$ on τ_{pd}. We note that since the p-channel threshold is low, $I^p_{D(sat)} >> I^n_{D(sat)}$ for the low V_{DD} used in our measurements, and hence τ_{pd} is determined mainly by $I^n_{D(sat)}$.

Plotted in Fig. 4.5 are measured and calculated composite delays versus f_s of the nine-stage inverter cascade at $V_{DD} = 1.5$ V with $V_{Gb} = \pm 10$ V. (Note that the substrate is the common back gate for the both the n- and p-channel MOSFETs). The delay, $\tau_D = 9\tau_{pd}$, was calculated using (4.21) for which $I^n_{D(sat)}$ was obtained from Fig. 4.4, accounting for the different Z/L. The measured dependences of τ_D (and τ_{pd}) on f_s and V_{Gb} are substantial and are in general accord with our analysis. At $V_{Gb} = +10$ V, τ_D is virtually independent of f_s because the overshoot

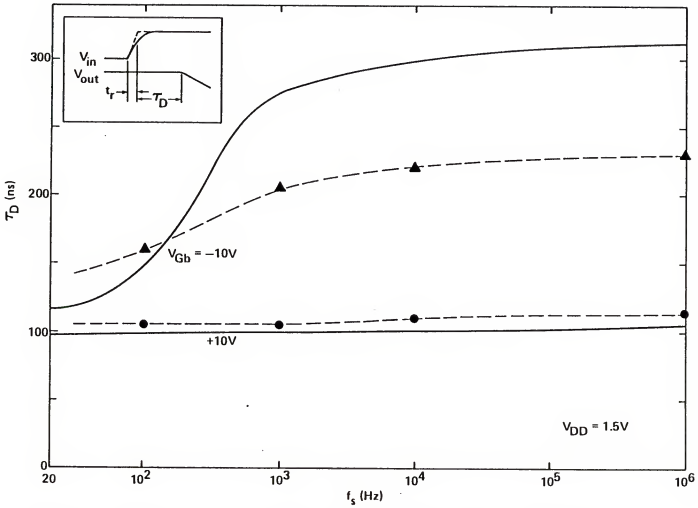

Figure 4.5 Measured (points) and calculated (solid lines) dependences on f_s of composite delay (τ_D) in a 9-stage SOI CMOS inverter cascade for V_{Gb} = ±10V. The inset shows how τ_D (= 9 τ_{pd}) was measured from the input and output voltage waveforms.

in $I^n_{D(sat)}$ is small relative to the steady-ON-state current, part of which is due to back-channel conduction. At V_{Gb} = - 10 V, τ_D is shorter at low f_s because of the significant overshoot in $I^n_{D(sat)}$. This dependence on f_s is overestimated by the theoretically based curve perhaps because of the inaccuracy in C_L in (4.21). Actually at high f_s, C_L is smaller than our assumed value because when the n-channel device is OFF, the charge in the floating body cannot change. Hence the gate capacitance is the series connection of C_{of}, C_b, and C_{ob}, which is much smaller than C_{of}. At low f_s however, the gate capacitance of the SOI MOSFET is larger and is defined similarly to that of the bulk MOSFET. (Note from Fig. 4.5 that $\tau_{pd} \sim 20$ nsec $< \tau_r$, which validates our use of (4.20) to theoretically estimate τ_{pd}.)

The results of Fig. 4.5 are for V_{DD} = 1.5 V. For higher V_{DD} ($\simeq$ 5 V), the overshoot in $I_{D(sat)}$ is small relative to the steady-state current as described in (4.3), and consequently the dependence of τ_{pd} on f_s is insignificant. However, the dependence of $I_{D(sat)}$, and hence of τ_{pd}, on V_{Gb} is significant irrespective of V_{DD}. For higher V_{DD}, $\tau_{pd}(V_{Gb})$ is implied by (4.21) and the steady-state current-voltage characteristics of the thin-film SOI MOSFET described in Chapter Three.

To study this dependence, we measured the oscillation frequency f_o of a 39-stage SOI CMOS ring oscillator at V_{DD} = 6 V for various values of V_{Gb}. The individual inverting stage is identical to that described previously. The propagation delay per stage, $\tau_{pd} = 1/2(39)f_o$ [56], is plotted versus V_{Gb} in Fig. 4.6. This measured τ_{pd} is consistent with (4.21) and our steady-state analysis. For $V_{Gb} > 0$, $I^n_{D(sat)} > I^p_{D(sat)}$ in

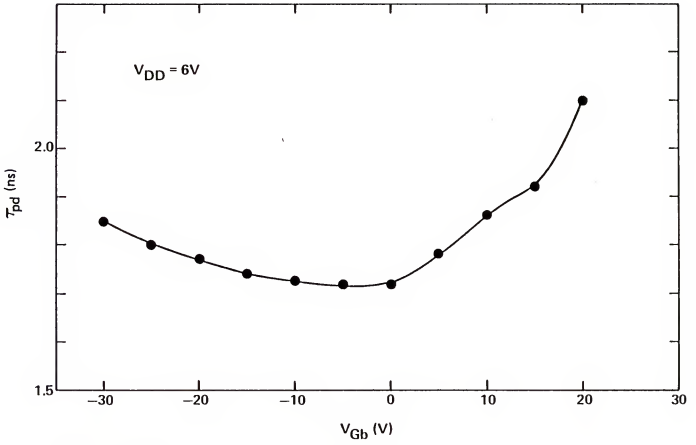

Figure 4.6 Measured dependence on V_{Gb} of propagation delay (τ_{pd}) per stage in a 39-stage SOI CMOS ring oscillator.

(4.21), and hence τ_{pd} is controlled mainly by $I^{p}_{D(sat)}$, which decreases with increasing V_{Gb}. For $V_{Gb} < -10$ V, the roles of the n- and p-channel devices are reversed. For $-10\ V < V_{Gb} < 0$, opposite dependences on V_{Gb} of $I^{n}_{D(sat)}$ and $I^{p}_{D(sat)}$ in (4.21) are compensating, and τ_{pd} is nearly insensitive to V_{Gb}. The steeper slope of the $\tau_{pd}(V_{Gb})$ curve for $V_{Gb} > 0$ reflects the stronger dependence of $I_{D(sat)}$ on V_{Gb} in the depletion-type p-channel transistor than in the deep-boron-implanted enhancement-mode n-channel transistor.

It should be noted that although the floating body, because of the overshoot in $I_{D(sat)}$, is advantageous with regard to τ_{pd} at low f_s ($\lesssim 1/\tau_G$), it can be detrimental at high f_s. It is clear from the charge expression derived in Chapter Five (i.e., (5.12.d)) that if $N_h \simeq 0$, which is typically true at high f_s, then when the back surface is accumulated, $\psi_{sb} \simeq V_B \propto (V_{Gf} - V_{DD})$ for $V^{A}_{Tf} < V_{Gf} < V_{DD}$. Thus V_B can be negative during the turn-ON, and hence the drive capability of the device is reduced and the switching speed is degraded. This detrimental floating-body effect is especially important when the rise time of the gate pulse is long, and C_L is small, such that the time needed to (dis)charge C_L is shorter than the rise time.

The detrimental effect is more significant when V_{DD} is high because a more negative V_B is developed, whereas the advantageous overshoot effect is less significant. As implied by our analysis, one way to avoid the detrimental floating-body effect is to bias the back gate so as to deplete the back surface. This bias (a higher V_{Gb}), in addition to ameliorating the detrimental effect, improves the current driving

capability of the device as described in Chapter Three. The back-surface leakage current, which would tend to increase in steady state, will be low when the device is switching because the negative going V_{Gf} pulse, which turns the device OFF, drives the back-surface potential to negative values.

4.4 Summary

Transient effects caused by the floating body of thin-film SOI MOSFETs have been analyzed, accounting for the charge coupling between the front and back gates. The transient drain current in the saturation region, which is directly related to the propagation delay of a digital circuit stage, has been modeled in terms of device and material parameters, switching frequency, and terminal voltages including the back-gate bias. The analysis was supported by measurements of transient $I_{D(sat)}$ in SOI MOSFETs fabricated in thin recrystallized silicon films. The measured dependences of the peak $I_{D(sat)}$ on f_s and V_{Gb} were well described by the analysis. SOI CMOS inverter cascades and ring oscillators were used to measure τ_{pd} versus f_s and V_{Gb}. A simple inverse relationship between τ_{pd} and the peak $I_{D(sat)}$ enabled explanations of these measured dependences based on the theoretical analysis of the transient $I_{D(sat)}$.

The theoretical-experimental results reveal that at low switching frequencies ($f_s \lesssim 1/\tau_G$), because of the overshoot in $I_{D(sat)}$, the floating body benefits the speed of SOI circuits. The relative significance of the overshoot current and its influence on τ_{pd} increase

with decreasing supply voltage, and hence the benefit is especially important in low-voltage circuits. For high f_s ($\gtrsim 1/\tau_G$), however, the floating body can degrade the speed of SOI circuits due to the negative body potential (V_B) prevalent during turn-ON. For very high f_s (~10 MHz), charge-pumping effects [57] in the floating body could further degrade the speed.

All of these floating-body effects are significant when the back surface is accumulated, but subside with increasing V_{Gb}. Implanting boron deep (near the back surface) into the n-channel device widens the range of V_{Gb} for which the floating-body effects are significant, and enhances the transient overshoot in $I_{D(sat)}$. In contrast, a boron implant at the front surface of the p-channel device, which renders the device depletion-mode, ameliorates the transient effects because the n-type region in the body remains depleted during switching due to the built-in potential of the p/n junction formed by the implant. These doping-profile dependences of the floating-body effects were confirmed by measurements of p- and n-channel devices having such doping profiles. Consequently, a stacked CMOS structure [14] comprising a depletion-type SOI device and an enhancement-type bulk device could possibly be designed to eliminate the frequency dependence of τ_{pd}, or to exploit the implied benefits to circuit speed.

CHAPTER FIVE
CHARGE-BASED MODEL AND EQUIVALENT CIRCUIT

5.1 Introduction

The device model needed for computer-aided analysis of SOI and 3-D MOS integrated circuits is completed by modeling, in addition to the source-drain transport current described in previous chapters, the transient currents that flow corresponding to the variation in terminal charges. In the conventional MOSFET model [30,40], a bias-dependent quasi-static capacitance between each terminal, assumed to be reciprocal, is used to account for the charging current at each terminal. This reciprocal-capacitance MOSFET model, although yielding correct results for most circuits when implemented in a circuit-simulation program, e.g., SPICE2 [58], is inadequate [36,37] for the simulation of some dynamic circuits because charge is not conserved in the model. The nonconservation of charge occurs because of inaccuracies in the representation of the underlying device physics, i.e., the neglect of the nonreciprocal properties of MOSFET capacitances [36,38], and because of improper numerical integration [36,37] of the charging currents into the bias-dependent capacitances in the simulation program. A resolution for this charge nonconservation problem is to calculate the charging current directly from the charge expressions instead of using capacitances [36,37].

In this chapter we describe the development of a charge-based large-signal model for the thin-film SOI MOSFET that accounts for the structural uniqueness. The intrinsic part of the device is of major concern here, but a brief guide to modeling the extrinsic part is also given. This model, developed for computer simulation of SOI and 3-D circuits, is based on the quasi-static approximation. Closed-form expressions for the terminal charges, continuous throughout the regions of operation, are derived in terms of terminal voltages and V_B for the two common back-surface charge conditions: depletion and accumulation. The linear relationship between the channel charge (areal) density Q_n and the front surface potential ψ_{sf}, obtained by assuming complete depletion of the film body, simplifies the charge expressions considerably and enables, following Ward [36], analytic partitioning of the channel charge into the source and drain charges.

A charge-based model is then described by expressing the terminal currents as time-derivatives of the charge expressions. The floating-body effects are accounted for in the model by including V_B in the terminal charge expressions and by including the current flow I_B into the body. The carrier generation and recombination in the body define I_B, which in turn defines the time-dependence of V_B. Possible simplification of the model for the case of negligible I_B is described.

To develop an equivalent circuit for the device, the charge-based terminal current expressions are expanded using the chain rule of differentiation to define charging currents flowing between each pair of terminals. The expansion coefficients, although having units of

capacitance, do not represent real capacitances in the device. They are nonreciprocal, depending on the channel charge partition between the source and the drain, with the exception of the front gate-back gate coefficient C_{GfGb}, which is reciprocal because of the complete-depletion condition in the body. The reciprocity in C_{GfGb} facilitates development of a simple equivalent circuit for the device in which all the capacitances are reciprocal and have positive values; all the nonreciprocities in the coefficients mentioned are removed through incorporation of the transient transport current I_{TT} that reflects the finite carrier transit delay in the channel. The analytic expression for I_{TT}, which can be obtained for the thin-film structure, enables the evaluation of the effective transit delay of the drain current in a saturated SOI MOSFET, and explains the charge nonconservation in the conventional reciprocal-capacitance MOSFET model [30,40].

5.2 Derivation of Charge Expressions

There are four principal (total) charge components in the intrinsic part of the SOI MOSFET enclosed by the dashed lines in Fig. 1.1: the front-gate charge Q_{Gf}, the inversion (channel) charge Q_N, the body charge Q_B, and the back-gate charge Q_{Gb}. These charges are related by the neutrality condition

$$Q_{Gf} + Q_N + Q_B + Q_{Gb} + ZL(Q_{ff} + Q_{fb}) = 0 \tag{5.1}$$

where Q_{ff} and Q_{fb} are the fixed charge densities at the front and back $Si\text{-}SiO_2$ interfaces. In (5.1) and in the charge model to be described, we neglect the surface-state charge at the front $Si\text{-}SiO_2$ interface because it can be small, and we do not include that at the back $Si\text{-}SiO_2$ interface for the following reasons. When the back surface is accumulated, the surface-state charge is fixed, independent of y and bias, and hence can be included in Q_{fb} effectively. When the back surface is depleted, the surface-state charge decreases with increasing V_{Gb} as we showed in Chapter Two, thereby widening the range of V_{Gb} in which the back surface is depleted. However, when the device is switched repeatedly, the trapped charge is nearly intact during a switching cycle since the carrier supply to the back surface is limited due to the finite carrier generation lifetime. Hence only very slow variations in V_{Gb} can cause significant changes in the surface-state charge. However such conditions are not common; V_{Gb} is usually fixed or changing (with V_{Gf}) rapidly.

The total charges can be obtained by integrating areal charge densities along the channel:

$$Q_{Gf} = Z \int_0^L C_{of}[V_{Gf} - \Phi_{MS}^f - \psi_{sf}(y)]dy \tag{5.2}$$

$$Q_N = Z \int_0^L Q_n(y)dy \tag{5.3}$$

$$Q_B = Z \int_0^L [Q_b + Q_{cb}(y)]dy \tag{5.4}$$

$$Q_{Gb} = Z \int_0^L C_{ob}[V_{Gb} - \phi_{MS}^b - \psi_{sb}(y)]dy \quad . \tag{5.5}$$

For the evaluation of (5.2)-(5.5), we use the quasi-static $Q_n(y)$ and $\psi_{sf}(y)$ derived in Appendix D. We simplify our model by considering only the two representative common back surface charge conditions: accumulation and depletion throughout the active region, which are the usual ones at $V_{Gb} = 0$ for p- and n-channel devices respectively. The linear relationship $Q_n(\psi_{sf})$ of the thin-film structure, in addition to providing the simple square-law characterization of the saturation drain current, greatly simplifies the charge expressions. We summarize below the results for the two common charge conditions at the back surface. To facilitate the systematic development of equivalent circuit, which we do later in this chapter, we include the source potential V_S in the charge expressions by defining other terminal voltages V_j relative to V_S: $V_{jS} = V_j - V_S$. (In the previous chapters we let $V_S = 0$, i.e., $V_{jS} \equiv V_j$.)

5.2.1 Depleted Back Surface

Since $Q_{cb}(y) \approx 0$, $Q_B = ZLQ_b$ is fixed, independent of the bias conditions. Then once Q_{Gf} and Q_N have been described, Q_{Gb} is obtained using the charge neutrality condition (5.1).

Triode Region $[V_{GfS} - V_{Tf} > (1 + \alpha)V_{DS}]$

$$Q_{Gf} = ZLC_{of}[V_{GfS} - \Phi_{MS}^{f} - 2\phi_B - \frac{V_{DS}}{2} + \frac{(1 + \alpha)V_{DS}^2}{12(V_{GfS} - V_{Tf} - \frac{(1+\alpha)}{2} V_{DS})}] \tag{5.6.a}$$

$$Q_N = -ZLC_{of}[V_{GfS} - V_{Tf} - \frac{(1+\alpha)}{2}V_{DS} + \frac{(1 + \alpha)^2V_{DS}^2}{12(V_{GfS} - V_{Tf} - \frac{(1+\alpha)}{2}V_{DS})}] \tag{5.6.b}$$

$$Q_{Gb} = ZLC_{bb}[V_{GbS} - \Phi_{MS}^{b} - \frac{Q_{fb}}{C_b} - 2\phi_B - \frac{Q_b}{2C_b} - \frac{V_{DS}}{2} + \frac{(1+\alpha)V_{DS}^2}{12(V_{GfS} - V_{Tf} - \frac{(1+\alpha)}{2}V_{DS})}] \quad . \tag{5.6.c}$$

Saturation Region $[0 < V_{GfS} - V_{Tf} < (1+\alpha)V_{DS}]$

$$Q_{Gf} = ZLC_{of}[V_{GfS} - \Phi_{MS}^{f} - 2\phi_B - \frac{(V_{GfS} - V_{Tf})}{3(1+\alpha)}] \tag{5.7.a}$$

$$Q_N = -ZLC_{of}(\frac{2}{3})(V_{GfS} - V_{Tf}) \tag{5.7.b}$$

$$Q_{Gb} = ZLC_{bb}[V_{GbS} - \Phi_{MS}^{f} - \frac{Q_{fb}}{C_b} - 2\phi_B - \frac{Q_b}{2C_b} - \frac{(V_{GfS} - V_{Tf})}{3(1+\alpha)}] \quad . \tag{5.7.c}$$

OFF Region $[V_{GfS} - V_{Tf} < 0]$

$$Q_{Gf} = ZLC_{fbb}[V_{GfS} - \Phi^f_{MS} - \frac{Q_{ff}}{C_{bb}} - \frac{Q_b}{2C_{bb}} - (V_{GbS} - V^b_{FB} + \frac{Q_b}{2C_{ob}})] \tag{5.8.a}$$

$$Q_N = 0 \tag{5.8.b}$$

$$Q_{Gb} = ZLC_{fbb}[V_{GbS} - \Phi^b_{MS} - \frac{Q_{fb}}{C_{fb}} - \frac{Q_b}{2C_{fb}} - (V_{GfS} - V^f_{FB} + \frac{Q_b}{2C_{of}})] \tag{5.8.c}$$

where

$$\frac{1}{C_{fbb}} \triangleq \frac{1}{C_{of}} + \frac{1}{C_b} + \frac{1}{C_{ob}} \tag{5.9}$$

and

$$\frac{1}{C_{fb}} \triangleq \frac{1}{C_{of}} + \frac{1}{C_b} \quad . \tag{5.10}$$

In the saturation region $[V_{DS} > V_{DS(sat)}]$, the charge expressions (5.7) were obtained by replacing V_{DS} in (5.6) with $V_{DS(sat)}$. In the OFF region, the expressions (5.8) followed after $\psi_{sf}(y)$ and $\psi_{sb}(y)$ were obtained from (3.3) and (3.4) with $Q_n(y) \simeq Q_{cb}(y) \simeq 0$. (We assume the film body remains completely depleted in the OFF region.)

5.2.2 Accumulated Back Surface

Since the expressions for $Q_n(y)$ and $\psi_{sf}(y)$ are applicable for both of the back-surface charge conditions if α and V_{Tf} are evaluated accordingly, the Q_{Gf} and Q_N expressions in (5.6) and (5.7) are also applicable to this case when the device is ON. The expression for Q_{Gb} is easily obtained from (5.5) with $\psi_{sb}(y) \simeq V_B$; then Q_B is defined by the charge neutrality condition (5.1). In the OFF region, Q_{Gf} is obtained from (5.2) with $\psi_{sf}(y)$ given by (3.3) with $Q_n(y) \simeq 0$ and $\psi_{sb}(y) \simeq V_B$.

Triode Region $[V_{GfS} - V_{Tf} > (1+\alpha)V_{DS}]$

$$Q_{Gf} \tag{5.11.a}$$

same as in (5.6)

$$Q_N \tag{5.11.b}$$

$$Q_{Gb} = ZLC_{ob}(V_{GbS} - \phi^b_{MS} - V_{BS}) \tag{5.11.c}$$

$$Q_B = -ZLC_{ob}\left[V_{GbS} - V^b_{FB} - \frac{Q_b}{2C_{ob}} - \left(1 + \frac{C_b}{C_{ob}}\right)V_{BS}\right. \tag{5.11.d}$$

$$\left. + \frac{C_b}{C_{ob}}\left(2\phi_B + \frac{V_{DS}}{2} - \frac{(1+\alpha)V^2_{DS}}{12\left(V_{GfS} - V_{Tf} - \frac{(1+\alpha)}{2}V_{DS}\right)}\right)\right] .$$

Saturation Region $[0 < V_{GfS} - V_{Tf} < (1+\alpha)V_{DS}]$

$$Q_{Gf} \tag{5.12.a}$$

same as in (5.7)

$$Q_N \tag{5.12.b}$$

$$Q_{Gb} = ZLC_{ob}(V_{GbS} - \Phi^b_{MS} - V_{BS}) \tag{5.12.c}$$

$$Q_B = -ZLC_{ob}[V_{GbS} - V^b_{FB} - \frac{Q_b}{2C_{ob}} - (1 + \frac{C_b}{C_{ob}})V_{BS} + \frac{C_b}{C_{ob}}(2\phi_B + \frac{V_{GfS} - V_{Tf}}{3(1+\alpha)})] \quad . \tag{5.12.d}$$

OFF Region $[V_{GfS} - V_{Tf} < 0]$

$$Q_{Gf} = ZLC_{fb}(V_{GfS} - \Phi^f_{MS} - \frac{Q_{ff}}{C_b} - \frac{Q_b}{2C_b} - V_{BS}) \tag{5.13.a}$$

$$Q_N = 0 \tag{5.13.b}$$

$$Q_{Gb} = ZLC_{ob}(V_{GbS} - \Phi^b_{MS} - V_{BS}) \tag{5.13.c}$$

$$Q_B = -ZLC_{fb}[V_{GfS} - V^f_{FB} + \frac{C_{ob}}{C_{fb}}(V_{GbS} - V^b_{FB}) - \frac{Q_b}{2C_b} - \frac{C_{ob}}{C_{fbb}}V_{BS}] \quad . \tag{5.13.d}$$

It should be noted that all the charge expressions are derived from the linear $Q_n(\psi_{sf})$ relationship in (3.3) and (3.4), which is based on

the assumption that the film body is completely depleted. Although the assumption might not be strictly valid for some specific cases, especially in the OFF region with the back surface accumulated if majority holes are supplied (generated) rapidly, extending the relationship to all regions of operation simplifies the model significantly while providing sufficient accuracy and ensuring continuity of the charge expressions throughout all regions of operation. Since the majority holes are supplied only through (thermal) carrier generation, the film body tends to remain depleted unless the OFF-time is sufficiently long. Even for a long OFF-time, during which the generated holes may neutralize ionized acceptor dopant atoms near the back surface as we described in Subsection 4.2.2, the depletion extension from the front surface at $V_{Gf} = 0$ can be comparable to the thickness of the thin-film body because of the large positive Q_{ff}. Generally then, any error resulting from the use of (3.3) and (3.4) in the OFF region is not significant.

5.2.3 Channel Charge Partition

We now partition the channel charge Q_N ($= Q_S + Q_D$) between the source (Q_S) and drain (Q_D). Ward [36], combining the carrier transport equation and the carrier continuity equation, showed that the currents flowing into the source and drain are, for strong inversion, given by

$$I_S(t) = \frac{dQ_S(t)}{dt} - I_o(t) \qquad (5.14.a)$$

and

$$I_D(t) = \frac{dQ_D(t)}{dt} + I_o(t) \tag{5.14.b}$$

where

$$I_o(t) = \frac{Z}{L} \int_o^L \mu_n \, |Q_n(y,t)| \, \frac{\partial \psi_{sf}(y,t)}{\partial y} \, dy \quad , \tag{5.15}$$

$$Q_S(t) = Z \int_o^L (1 - \frac{y}{L}) \, Q_n(y,t) \, dy \quad , \tag{5.16.a}$$

and

$$Q_D(t) = Z \int_o^L \frac{y}{L} \, Q_n(y,t) \, dy \quad . \tag{5.16.b}$$

In the quasi-steady-state, $I_o(t)$ is given by the steady-state drain current equation including time-varying terminal voltages, and $Q_S(t)$ and $Q_D(t)$ are evaluated by using the quasi-static $Q_n(y)$ in (D.6):

$$I_o = \frac{Z}{L} \mu_n C_{of} \left[(V_{GfS} - V_{Tf}) V_{DS} - (1 + \alpha) \frac{V_{DS}^2}{2} \right] \quad ; \tag{5.17}$$

$$Q_S = -\frac{2}{3} ZLC_{of}(1 + \alpha) V_{DS} \left[\frac{u^3}{2u - 1} - \frac{2}{5} \frac{u^5 - (u - 1)^5}{(2u - 1)^2} \right] \tag{5.18.a}$$

and

$$Q_D = -\frac{2}{3} ZLC_{of}(1 + \alpha)V_{DS}\left[-\frac{(u - 1)^3}{2u - 1} + \frac{2}{5}\frac{u^5 - (u - 1)^5}{(2u - 1)^2}\right] \qquad (5.18.b)$$

where

$$u \triangleq \frac{V_{GfS} - V_{Tf}}{(1 + \alpha)V_{DS}} \quad . \qquad (5.19)$$

The parameter u reflects the region of operation. In the saturation region, $u = 1$ ($V_{DS} \geq V_{DS(sat)}$), and $Q_S = (3/5)Q_N$ and $Q_D = (2/5)Q_N$; in the linear region, u is very large, and $Q_S \approx Q_D \approx Q_N/2$; Q_N is given by (5.6.b), (5.7.b), (5.11.b), or (5.12.b). Note that these results apply for both charge conditions at the back surface, provided α and V_{Tf} are evaluated properly.

The prediction of a non-zero Q_D in the saturation region is physically unrealistic. It resulted from modeling the transport current in the channel by $I_o(t)$ in (5.15), which is simply the average channel current. Although physically unrealistic, this model is convenient in the quasi-steady-state because (5.17) derives, and it does yield accurate terminal characteristics. The inaccuracy of equating I_o in (5.17) to the transport current is negated by the unrealistic charge partitioning in (5.18). In Section 5.4 we discuss how the model can be made more physically realistic by accounting for the transient component of the transport current that reflects the finite carrier transit delay in the channel.

Note that contrasted to the bulk MOSFET [36], the expressions for Q_S and Q_D are closed-form, yet fully account for the body effects. This

simplifying feature of the SOI MOSFET is afforded by the linear $Q_n(\psi_{sf})$ relationship, due to the limiting of the depletion-region extension by the back oxide. Since the charge expressions are closed-form and are continuous throughout the regions of operation, the model provides a basis for efficient computer-aided analysis of SOI and 3-D circuits with charge conservation ensured.

5.3. Charge-Based Model

With the source-drain transport current model I_o in (5.17), the derived charge expressions in Section 5.2 provide a complete charge-based large-signal model of the intrinsic SOI MOSFET operating in the quasi-steady-state. When the back surface is depleted, the floating-body effects are negligible since Q_B does not vary in time appreciably from the depletion charge ZLQ_b; majority holes are quickly swept out of the body. Consequently, as shown in Section 5.2, all charge and current expressions are completely defined by the four terminal voltages. Neglecting the source-drain leakage current, we express the currents flowing into the terminals by (5.14), and

$$I_{Gf}(t) = \frac{dQ_{Gf}(t)}{dt} \tag{5.20}$$

and

$$I_{Gb}(t) = \frac{dQ_{Gb}(t)}{dt} \quad . \tag{5.21}$$

When the back surface is accumulated, the floating-body effects can be important; the charges and currents are defined by, in addition to the four terminal voltages, $V_B(t)$, which can have arbitrary value for transient conditions depending on $Q_B(t)$. The transient overshoot in the drain current at low switching frequency, which is accounted for in the model via $V_B(t)$ and $Q_B(t)$, exemplifies the significance of the floating-body effects. The charge-based model for this case is completed by regarding the body (accumulation layer) as an independent terminal and defining the body current $I_B(t)$, which in turn defines $Q_B(t)$ and hence $V_B(t)$. Modeling the carrier generation and recombination in the floating body defines $I_B(t)$.

The generation current I_G flows from the drain to the body since, after hole-electron pair generation in the body, holes are attracted to the back accumulation layer whereas electrons are swept to the drain. Approximating the time-varying depletion-region width by t_b, (4.4) gives

$$I_G \simeq qGZLt_b \tag{5.22}$$

The recombination current I_R flows from the body to the source because recombination of majority holes occurs predominantly at the forward-biased source-body junction. From (4.18)

$$I_R \simeq qZt_bW_{SCR}\left(\frac{n_i}{\tau_r}\right)\exp\left(\frac{qV_{BS}}{2kT}\right) \tag{5.23}$$

The terminal currents that account for the variation in the body charge are thus

$$I_S(t) = \frac{dQ_S(t)}{dt} - I_o(t) - I_R(t) \qquad (5.24.a)$$

and

$$I_D(t) = \frac{dQ_D(t)}{dt} + I_o(t) + I_G(t) \quad ; \qquad (5.24.b)$$

the gate currents are still given by (5.20) and (5.21). Finally, to complete the description of the transient voltage and current at each terminal, we express

$$I_B(t) = \frac{dQ_B(t)}{dt} = I_G(t) - I_R(t) \quad , \qquad (5.25)$$

which defines $V_B(t)$. Note that the initial value of V_B for a transient analysis is defined by the steady-state condition $I_B = 0$.

A simplification of the general model could be made by neglecting the time dependence of $Q_B(t)$, i.e., by letting $I_B(t) \simeq 0$. With a fixed Q_B, all charges and currents are described by the four terminal voltages when V_{BS} is derived from $Q_B(V_{Gf}, V_{Gb}, V_D, V_S, V_B)$ in (5.11.d), (5.12.d), or (5.13.d), and inserted into the expressions for external terminal charges and drain current. Then the floating-body effects, subject to a nearly time-independent Q_B, are accounted for implicitly in the four-terminal model.

The fixed-Q_B assumption is valid for most transient conditions; it is valid unless the OFF-time t_{off} is long enough such that $t_{off}I_G \sim ZLQ_b$. (We can see from Fig. 4.4 that for the typical SOI MOSFET we measured in Chapter Four, $t_{off}I_G \sim ZLQ_b$ when the switching frequency is $\sim$ 100 Hz.) The value of the fixed Q_B for the short-t_{off} case can be evaluated in the saturation region at $V_{GfS} = V_{DD}$ (the supply voltage), where V_B and hence I_R are maximum. Because I_R varies exponentially with V_{BS} and I_G ($\simeq I_R$) is limited by thermal carrier generation, $V_{BS} \simeq 0$. Then Q_B follows directly from (5.12.d), and represents an average value about which only small transient variations occur; also, $I_G \simeq I_R \simeq 0$.

The charge-based model described in this section can be reliably implemented in a circuit simulator, e.g., SPICE2 [58], in a way similar to that suggested in [36] and [37]. Both current and charge conservation at the terminals is ensured because all the charge expressions incorporate the charge neutrality condition (5.1), and they are continuous throughout all regions of operation.

5.4 Equivalent Circuit

Although the charge-based model describes completely the large-signal behavior of the SOI MOSFET, a better physical insight into the device can be facilitated by an equivalent circuit. In addition, the equivalent circuit enables computer simulation of SOI and 3-D MOS integrated circuits using existing simulator programs, e.g, SPICE2 [58], without any significant revision, which is required to use the charge-based model [36,37].

5.4.1 Depleted Back Surface

We first develop the equivalent circuit for the depleted back surface case, in which the floating-body effects are negligible. Since all the terminal charges are described completely in terms of the four terminal voltages, expanding their time-derivatives by the chain rule of differentiation gives the terminal charging currents as

$$I_i^C = \frac{dQ_i}{dt} = - \sum_j C_{ij} \frac{dV_j}{dt} \tag{5.26}$$

where

$$C_{ij} = - \frac{\partial Q_i}{\partial V_j} \quad ; \tag{5.27}$$

in (5.26) and (5.27), i,j = Gf, Gb, D, S. Note that (5.26) is simply a mathematical expansion and hence the coefficients C_{ij}, although having the unit of capacitance, do not represent any real capacitances in the device. It is not surprising then that they can be nonreciprocal, i.e., $C_{ij} \neq C_{ji}$.

To describe the terminal currents by circuit components, we first redefine C_{ii} in (5.26) by incorporating the charge neutrality condition:

$$C_{ii} = - \sum_{j \neq i} C_{ji} \quad . \tag{5.28}$$

Then combining (5.26) and (5.28) yields

$$I_i^c = \sum_{j \neq i} I_{ij} \tag{5.29}$$

where

$$I_{ij} = -C_{ij} \frac{dV_j}{dt} + C_{ji} \frac{dV_i}{dt}$$

$$\equiv C_{ij} \frac{dV_{ij}}{dt} - (C_{ij} - C_{ji}) \frac{dV_i}{dt} \quad . \tag{5.30}$$

Note that the first term in (5.30) can be represented by a real reciprocal capacitor C_{ij}, whereas the second term is a transcapacitive current flowing from terminal i to terminal j. Hence the equivalent circuit is represented by, in addition to the source-drain quasi-static transport current I_o, the parallel combination of the reciprocal capacitor and the transcapacitive current source between each pair of terminals.

This basic equivalent circuit for the four-terminal SOI MOSFET is shown in Fig. 5.1. We summarize in Table 5.1 the expressions for C_{ij} derived from (5.27) using the charge expressions developed in Section 5.2. A noteworthy result is that the ratio of all the C_{ij} associated with the front gate (i.e., i,j = Gf) to the corresponding C_{ij} associated with the back gate is a constant, independent of the bias conditions:

$$\frac{C_{GbS}}{C_{GfS}} = \frac{C_{GbD}}{C_{GfD}} = \frac{C_{SGb}}{C_{SGf}} = \frac{C_{DGb}}{C_{DGf}} = \alpha \quad \left(= \frac{C_{bb}}{C_{of}}\right) \quad . \tag{5.31}$$

Table 5.1 Summary of C_{ij} (Depleted Back Surface: $\alpha = C_{bb}/C_{of}$)

C_{ij}	Triode Region	Saturation Region	OFF Region
$C_{GfGb} = C_{GbGf}$	$ZLC_{fbb}\left[\frac{1}{3(2u-1)^2}\right]$	$ZL\frac{C_{fbb}}{3}$	ZLC_{fbb}
C_{GfS}	$ZLC_{of}\left[\frac{6u^2-4u}{3(2u-1)^2}\right]$	$ZLC_{of}\frac{2}{3}$	0
C_{SGf}	$ZLC_{of}\left[\frac{12u^3-18u^2+8u-\frac{4}{5}}{3(2u-1)^3}\right]$	$ZLC_{of}\frac{2}{5}$	0
C_{GfD}	$ZLC_{of}\left[\frac{6u^2-8u+2}{3(2u-1)^2}\right]$	0	0
C_{DGf}	$ZLC_{of}\left[\frac{12u^3-18u^2+8u-\frac{6}{5}}{3(2u-1)^3}\right]$	$ZLC_{of}\frac{4}{15}$	0
C_{SD}	$ZLC_{of}(1+\alpha)\left[\frac{-4u^3+8u^2-\frac{24}{5}u+\frac{4}{5}}{3(2u-1)^2}\right]$	0	0
C_{DS}	$ZLC_{of}(1+\alpha)\left[\frac{-4u^3+4u^2-\frac{4}{5}u}{3(2u-1)^2}\right]$	$-ZLC_{of}(1+\alpha)\frac{4}{15}$	0
C_{GbS}	αC_{GfS}		
C_{SGb}	αC_{SGf}		
C_{GbD}	αC_{GfD}		
C_{DGb}	αC_{DGf}		

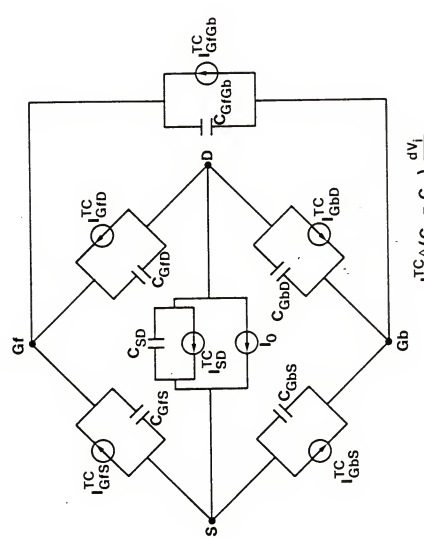

Figure 5.1 General equivalent circuit of SOI MOSFET having depleted back surface.

This constant ratio can be explained physically. Because of the complete depletion of the film body, at any position in the channel the capacitance between the channel and back gate is fixed at C_{bb}, the series capacitance of the depleted film and the back oxide. A similar relationship has been modeled for the bulk MOSFET [38,59], but due to the bias-dependent body capacitance, the bulk MOSFET ratio corresponding to (5.31) is bias-dependent and the equalities are only approximate.

Another important characteristic of the thin-film device is that the transcapacitive current between the front and back gate is zero; i.e., C_{GfGb} is reciprocal as indicated in Table 5.1. This reciprocity simplifies the equivalent circuit significantly because, in addition to removing the transcapacitive current source between the two gates, it enables the unification of all the gate transcapacitive currents into a source-drain transient transport current. Using the reciprocity, (5.28), and [38]

$$\sum_j C_{ij} \equiv 0 \quad , \tag{5.32}$$

which follows from that fact that all Q_i are given by the terminal voltages relative to V_S, we can show that the transcapacitive currents directed to the front gate from the source and the drain have the same magnitude but opposite signs; i.e., $C_{GfS} - C_{SGf} = -(C_{GfD} - C_{DGf})$. Since a similar relationship obtains for the back gate also, we can effectively remove all the transcapacitive current sources flowing into the gates by connecting them between the source and drain.

We show in Fig. 5.2 the resulting simplfied large-signal equivalent circuit for the intrinsic thin-film SOI MOSFET having a depleted back surface. The quasi-static equivalent circuit includes reciprocal positive capacitances, the quasi-static source-drain transport current I_o, and a transient transport current I_{TT}. The I_{TT} includes previously mentioned front- and back-gate transcapacitive currents as well as the current flow due to the negative, nonreciprocal source-drain capacitance included in Fig. 5.1:

$$I_{TT} = (C_{GfD} - C_{DGf}) \frac{dV_{Gf}}{dt} + (C_{GbD} - C_{DGb}) \frac{dV_{Gb}}{dt}$$

$$+ (C_{SD} - C_{DS}) \frac{dV_S}{dt} + C_{SD} \frac{dV_{DS}}{dt} \quad . \tag{5.33}$$

From Table I, we find $(C_{GfD} - C_{DGf}) = (C_{GbD} - C_{DGb})/\alpha = -(C_{SD} - C_{DS})/(1 + \alpha)$; noting from (2.12) that $\alpha dV_{GbS}/dt = -dV_{Tf}/dt$ when $C_{sb} \simeq 0$, we thus have

$$I_{TT} = C_{TT} \frac{d(V_{GfS} - V_{Tf})}{dt} + C_{SD} \frac{dV_{DS}}{dt} \tag{5.34}$$

where

$$C_{TT} = -ZLC_{of} \left[\frac{4u^2 - 4u + \frac{4}{5}}{3(2u - 1)^3}\right] \tag{5.35}$$

and C_{SD} (< 0) is defined in Table 5.1. When the device is in the saturation region, $C_{TT} = -ZLC_{of}(4/15)$ and $C_{SD} = 0$.

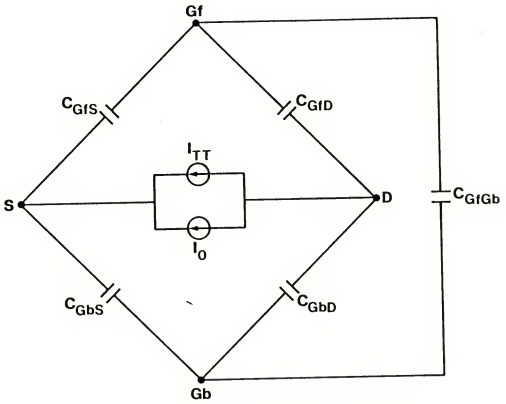

Figure 5.2 Simplified representation of equivalent circuit in Fig. 5.1 resulting from incorporating all the transcapacitive current sources into I_{TT}.

The physical origin of this negative (opposite to I_o) I_{TT} is the finite carrier transit delay through the channel. This becomes obvious when we note that I_{TT} in Fig. 5.2 is the only addition to the conventional reciprocal-capacitance MOSFET model [30,40], which does not account for the delay. Even in the quasi-steady-state, due to the transmission-line effects [52,53], the actual transport current has a finite time lag from I_o. We assess in the Appendix E the significance of I_{TT} with regard to transient analysis of MOS integrated circuits. The effects of I_{TT} on charge conservation and circuit delay are evaluated by deriving the negative transport charge implied by I_{TT} and the corresponding average delay in the drain current. We find I_{TT} to be important for dielectrically isolated devices in which the intrinsic capacitances are the predominant charge-storing components.

To indicate relative magnitudes and bias dependences of the capacitances in the equivalent circuit in Fig. 5.2, we plot in Fig. 5.3 the capacitances for a typical SOI MOSFET versus a normalized gate voltage (u in the triode region). Plots of C_{TT} and C_{SD} are included to show the significance of I_{TT} relative to the charging currents. We note that the capacitances associated with the back gate are relatively small in all regions of operation, whereas C_{GfS} is predominant. In the triode region, C_{GfD} becomes significant as V_{GfS} increases, as does C_{SD}.

5.4.2 Accumulated Back Surface

For the accumulated case, the body (accumulation layer) is regarded as an effective terminal to account for the floating-body effects. We

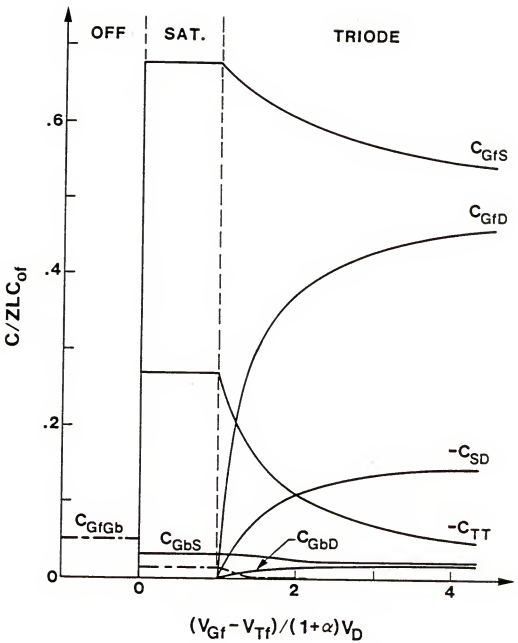

Figure 5.3 Normalized bias dependences of the equivalent-circuit capacitances in Fig. 5.2 for a typical device having t_{of} = 500 Å, t_{ob} = 8000 Å, and t_b = 4000 Å.

summarize in Table 5.2 the capacitances between each terminal, derived similarly to those in Table 5.1 using the appropriate charge expressions in Section 5.2. Because the accumulation layer has a uniform potential, and the capacitance between it and the channel throughout the intrinsic part of the device is fixed at C_b, independent of V_D, the capacitances between the body and the two gates are reciprocal. Also, for the same reason, all the source and drain capacitances are expressed identically to the corresponding ones in Table 5.1, if the body terminal replaces the back-gate terminal (and now $\alpha = C_b/C_{of}$). A similar conversion to the reciprocal network is hence possible and I_{TT} is again given by (5.34).

We show in Fig. 5.4 the resulting equivalent circuit. The storage of generated holes in the body and their recombination are accounted for by connecting a current source I_G and a diode (with forward current I_R) at the body-drain and at the body-source junctions respectively. The models for I_G and the diode current I_R are given in (5.22) and (5.23). For the case of significant carrier generation by impact ionization near the drain, the model for I_G should include the avalanching current component [27], in addition to thermal generation modeled in (5.22). This would account for the "kink" [24,27] in the steady-state $I_D(V_D)$ characteristic.

To illustrate the effect of the back-surface charge condition, we plot in Fig. 5.5 C_{GfS} and C_{GfD} versus V_{GfS} for the two charge conditions in the same device used in Fig. 5.3 at $V_{DS} = 1V$. The differences between the two cases are defined by the difference in α in (D.8),

Table 5.2 Summary of C_{ij} (Accumulated Back Surface: $\alpha = C_b/C_{of}$)

C_{ij}	Triode Region	Saturation Region	OFF Region
$C_{GfB} = C_{BGf}$	$ZLC_{fb}\left[\frac{1}{3(2u-1)^2}\right]$	$ZL\frac{C_{fb}}{3}$	ZLC_{fb}
$C_{GbB} = C_{BGb}$	ZLC_{ob}	ZLC_{ob}	ZLC_{ob}
C_{GfS} C_{SGf} C_{GfD} C_{DGf} C_{SD} C_{DS}		Same as in Table I	
C_{BS}		αC_{GfS}	
C_{SB}		αC_{SGf}	
C_{BD}		αC_{GfD}	
C_{DB}		αC_{DGf}	

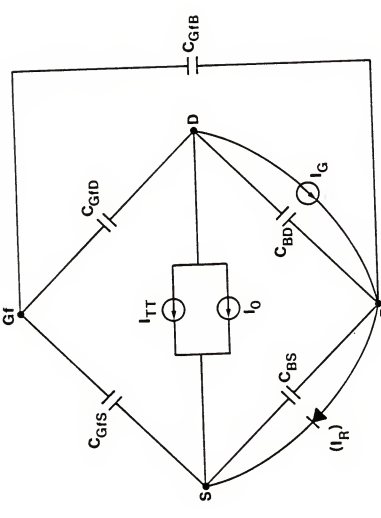

Figure 5.4 Equivalent circuit of SOI MOSFET having accumulated back surface. The diode (I_R) and the current source I_G represent the carrier recombination and generation in the body respectively.

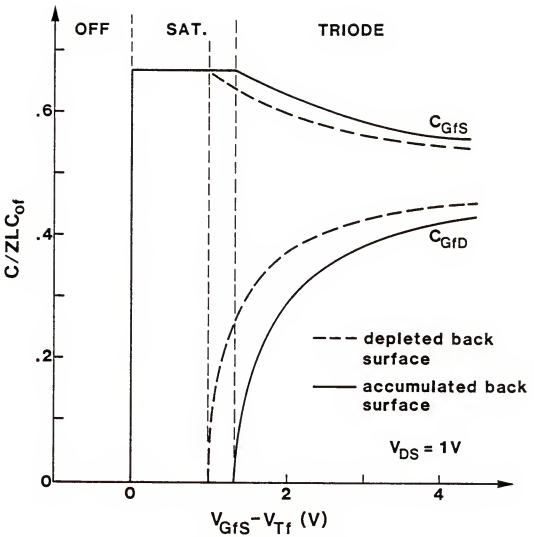

Figure 5.5 Normalized bias dependence of C_{GfS} and C_{GfD} for different back surface charge conditions in the same device used in Fig. 5.3.

which, for example, produces the difference in $V_{DS(sat)}$ defined by (D.11).

5.4.3 Simpler Equivalent Circuits

As evidenced by the the capacitance plots in Fig. 5.3, the back oxide in a typical SOI MOSFET is sufficiently thick such that $C_{ob} \ll C_b$, C_{of}, which renders C_{GbS}, C_{GbD}, and C_{GbGf} relatively small. For this case, the equivalent circuit is simplfied considerably. When the back surface is depleted, the simpler equivalent circuit is that in Fig. 5.2 with $C_{GbS} \approx C_{GbD} \approx C_{GbGf} \approx 0$, which has only three terminals. When the back surface is accumulated, it is that in Fig. 5.4 with $C_{GbB} \approx 0$.

For the accumulated back surface case, the equivalent circuit is further simplfied when Q_B can be assumed fixed, i.e., when $I_G \approx I_R \approx 0$. The equivalent circuit in Fig. 5.4 can then be reduced, as illustrated in Fig. 5.6, to a three-terminal network by converting the loop-form circuit of C_{BS}, C_{BD}, and C_{GfB} into nodal form [60]. The capacitances in the simplified equivalent circuit (Fig. 5.6(c)) are summarized in Table 5.3. Since $C'_{GfS} \approx C_{GfS}$, $C'_{GfD} \approx G_{GfD}$, and $C'_{SD} \approx 0$ for a typical device, the main floating-body effects follow from the dependence of I_o on a variable V_B, which is implicitly accounted for, through (4.2) and (5.17), in the circuit. The simple equivalent circuit in Fig. 5.6(c) thus applies to the depleted-back-surface case discussed above as well, provided the capacitances are defined appropriately as illustrated in Fig. 5.5.

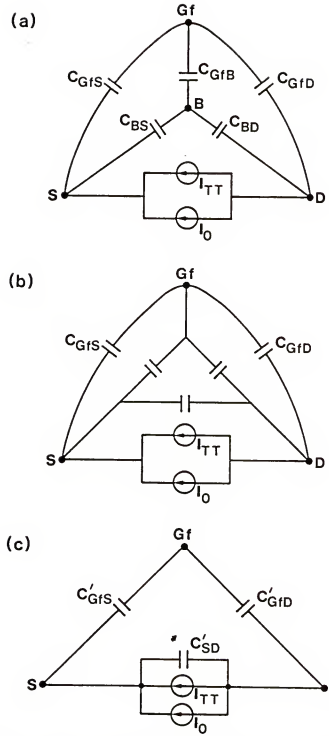

Figure 5.6 Simplification of the equivalent circuit in Fig. 5.4 when the back oxide is thick ($C_{GbB} \approx 0$) and the body charge is nearly fixed ($I_R \approx I_G \approx 0$). For these conditions the circuit in Fig. 5.4 reduces to that in (a), which transforms to that in (b) when the capacitor loop-form circuit is converted to its nodal form. Adding the parallel capacitances in (b) yields the simplified three-terminal equivalent circuit in (c).

Table 5.3 Expressions for Capacitances in Fig. 5.6

($\alpha = C_b/C_{of}$)

Capacitances	Triode Region	Saturation Region	OFF Region
$C'_{GfS} = G_{GfS} + \frac{C_{BS}C_{GfB}}{C_{BS}+C_{BD}+C_{GfB}}$	$ZLC_{of}\frac{6u^2-4u}{3(2u-1)^2}\left(1 + \frac{\alpha}{(1+\alpha)(12u^2-12u+2)+1}\right)$	$ZLC_{of}\frac{2(1+\alpha)}{3+2\alpha}$	0
$C'_{GfD} = C_{GfD} + \frac{C_{BD}C_{GfB}}{C_{BS}+C_{BD}+C_{GfB}}$	$ZLC_{of}\frac{6u^2-8u+2}{3(2u-1)^2}\left(1 + \frac{\alpha}{(1+\alpha)(12u^2-12u+2)+1}\right)$	0	0
$C'_{SD} = \frac{C_{BS}C_{BD}}{C_{BS}+C_{BD}+C_{GfB}}$	$ZLC_{of}\frac{6u^2-8u+2}{3(2u-1)^2}\left(\frac{\alpha(1+\alpha)(6u^2-4u)}{(1+\alpha)(12u^2-12u+2)+1}\right)$	0	0

5.4.4 Extrinsic Capacitances

To be useful for circuit simulation, the intrinsic equivalent circuit must be supplemented with the extrinsic device model. There are three primary extrinsic capacitances at the drain (and at the source) of the SOI MOSFET (see Fig. 1.1): capacitances connected to the front gate, the back gate, and the body. The capacitance between the drain and the front gate is predominantly the gate-oxide overlap capacitance, which is identical to that in the bulk MOSFET [30]. The drain to back-gate capacitance is simply the back-oxide capacitance under the drain. The drain-body capacitance is dependent on the back-surface charge condition and can be characterized by a complicated two-dimensional field analysis. However the capacitance is typically very small because the film body is depleted. When the back surface is depleted, the lateral electric field flux from the drain will terminate at the back gate, which adds small fringing effects to the drain-back gate capacitance. When the back surface is accumulated, although there exists a finite capacitance between the body (accumulaton layer) and drain, the capacitance is small because the accumulation layer is thin.

5.5 Summary

We have developed a charge-based large-signal model for the thin-film SOI MOSFET, emphasizing the unique features that distinguish it from the bulk counterpart. Closed-form expressions for the terminal charges, derived using the quasi-static approximation, are used to define the terminal currents. The effects of the thin and floating

body, along with those of back-gate biasing through the thin underlying oxide, are explicitly accounted for in the model. Since the derived charge expressions are given in simple closed form and are continuous throughout the regions of operation, the model is useful for computer-aided transient analysis of SOI and 3-D circuits when implemented in a simulation program, e.g., SPICE2.

An equivalent circuit of the device was developed from the charge-conserving model. The device is represented by real reciprocal capacitances, a quasi-static transport current, and a transient transport current that reflects the finite carrier transit delay in the channel. The equivalent circuit is simpler than that for the bulk MOSFET because C_{GfGb} is reciprocal, due to the thin-film structure. The analytic expression for the transient transport current enables the evaluation of the nonconservation of charge in the conventional reciprocal-capacitance model, and facilitates the evaluation of the average carrier transit delay in the channel (see Appendix E).

CHAPTER SIX
SUMMARY, CONCLUSIONS, AND RECOMMENDATIONS

6.1 Summary and Conclusions

We have described the development of analytic models for threshold voltage, drain current, and terminal charges (capacitances) of thin-film SOI MOSFETs, emphasizing the unique features of the devices that distinguish them from their bulk counterparts. The modulation of the front-channel conductance by the back-gate bias, and the coupling of the floating-body potential with the external voltages in the steady-state and transient conditions are explicitly accounted for in the developed models. The limiting of the depletion-region extension by the underlying oxide simplifies the device models considerably and renders them useful for SOI device design as well as for SOI circuit simulation.

In Chapter Two, we have done a one-dimensional analysis of the charge coupling between the front and back gates in thin-film SOI MOSFETs, and derived closed-form expressions for the (front-gate) threshold voltage under all possible steady-state conditions. The expressions clearly show the dependence of the threshold voltage on the back-gate bias and on the device parameters, including those of the back silicon-insulator interface as well as thickness and doping density of film body. The analysis is supported by linear-region current-voltage

measurements of laser-recrystallized SOI MOSFETs. The results suggest how the back-gate bias may be used to optimize the performance of the SOI MOSFET in particular applications. For example, accumulating the back surface, despite reducing the current deriving capability, suppresses the back- surface leakage current as well as the sensitivity of V_{Tf} on the device parameters.

In Chapter Three, a simple analytic model for the steady-state current-voltage characteristics of strongly inverted thin-film SOI MOSFETs was developed. The model, simplified by a key approximation that the inversion charge density is described well by a linear function of the surface potential, clearly shows the dependence of the drain current on the device parameters and on the terminal voltages, including the back-gate (substrate) bias. Because of the thin-film structure, the drain current expressions are simpler than those of bulk MOSFETs when the charge condition at the back surface is uniform throughout the active region. The analysis is supported by measurements of current-voltage characteristics of thin-film (laser-recrystallized) SOI MOSFETs. The dependence of carrier mobility on the terminal voltages, especially the back-gate bias, is analyzed and shown to underlie discrepancies between the theoretical (constant mobility) and experimental results at high gate voltages. The mobility dependence on the back-gate bias enhances the strong influence of the back gate on the drain current, especially when the device is saturated.

In Chapter Four, we have analyzed the effects of the floating body on the transient drain current of four-terminal thin-film SOI MOSFETs,

and assessed their influence on propagation delay (speed) in SOI CMOS digital circuits. The analysis accounts for the charge coupling between the front and back gates, and hence describes the dependence of the transient drain (saturation) current and propagation delay on the back-gate bias as well as on the switching frequency. Measurements of the transient current in recrystallized SOI MOSFETs and of propagation delay in SOI CMOS inverters and ring oscillators for various switching frequencies are described and shown to support the theoretical analysis. The floating body is beneficial in low-voltage low-frequency circuits, although at high frequencies it can degrade the circuit speed, especially at high supply voltage.

A charge-based large-signal model for thin-film SOI MOSFETs, intended for computer simulation of transient characteristics of SOI and 3-D circuits, has been developed in Chapter Five, based on the quasi-static approximation. Closed-form expressions for the terminal charges, simpler than those for the bulk MOSFET because of the thin-film structure, are derived in terms of terminal voltages and device parameters, and are used to define the terminal currents. The charge-based model accounts for the important structural uniqueness, i.e., it includes the effects of the thin, floating body and the back-gate biasing. We then showed, by expanding the charging current using the chain rule, that the device can be accurately represented using only real reciprocal capacitances with the inclusion of the transient channel transport current I_{TT}. The analytic expression for I_{TT}, obtainable for the thin-film structure, enables the evaluation of the average carrier

transit delay in the channel and of the corresponding charge nonconservation in the conventional reciprocal-capacitance MOSFET model that does not account for the delay.

6.2 Recommendations for Further Research

First, we recommend computer simulation of SOI and 3-D basic circuits, e.g., CMOS inverters, having various structures [10-16]. The effects of intra- and inter-device (capacitive) coupling on the steady-state transfer characteristics as well as on the transient response of CMOS inverters can be simulated by incorporating the developed intrinsic charge-based model into circuit simulation programs, e.g., SPICE2 [58], and supplementing it with models for external capacitances, which are typically simple oxide capacitances. Comparison of simulation results for various structures could be used in the optimization of CMOS structures for each specific application. The degradation in circuit speed, expected in 3-D circuits because of the inter-device coupling, can also be estimated from the simulation.

Second, we recommend modeling of the subthreshold conduction in SOI MOSFETs. Recently proposed one-transistor dynamic RAM cells employing an SOI MOSFET as the access transistor show prolonged storage time as well as improved tolerance against soft errors [61,62]. Since the charge retention in these cells is limited by the leakage current of the access transistor, characterization of the subthreshold conduction in the SOI MOSFET is indispensable for successful application of SOI technologies to dynamic memory circuits. The characterizations of the

leakage current in SOI devcies should include the effects of the back-surface conduction as well as the dependences of the front-channel subthreshold conduction on V_{Gb} and on the back $Si\text{-}SiO_2$ interface properties [46]. These effects can be minimized by accumulating the back surface strongly. The possible presence of grain boundaries in the recrystallized silicon film, which have significant effects on the channel conductance in moderate and weak-inversion regions [63], also needs to be accounted for in the subthreshold drain current model. The surface states at both the front and back $Si\text{-}SiO_2$ interfaces are important for the subthreshold characteristics of SOI devices and deserve a comprehensive investigation. The diffusion and drift of carriers are comparable to each other [50] in the moderate-inversion region [43], and hence should be included in a generalized characterization of leakage current.

Third, we recommend modeling of small-geometry effects in the SOI MOSFET, which is essential in the development SOI VLSI. Major small-geometry effects in a scaled-down [64] bulk device include (1) the depletion-charge sharing between source, drain, and gate, which results in the dependence of threshold voltage on device size [65], (2) the lowering of the channel surface potential by the depletion extension from the drain at high drain voltage [66], which increases the OFF-state leakage current, (3) the saturation of carrier drift velocity along the channel due to high lateral electric field, which reduces the saturation drain voltage as well as the drain current [67]. All these effects should be remodeled accounting for the limiting of depletion region

extension by underlying oxide and for the control of the back-surface charge condition by the back-gate biasing. Accumulating the back surface will minimize the first two small-geometry effects because the electric field perpendicular to the channel is stronger and hence the lateral electric field from the drain is weaker (relative to the total field).

Fourth, we recommend further studies on the detrimental effects of the floating body at high switching frequencies, discussed briefly in Chapter Four. The body potential in transient conditions, which is defined by the transient body charges relative to the steady-state ones, can be negative because of the excessive recombination of the majority holes in the body (n-channel device) with the electrons injected from 1) the source when the source-body junction is forward biased in the ON state, and 2) the channel after abrupt turn-OFF. The first effect causes a negative body potential during the turn-ON as we indicated in Section 4.3. The second effect, the charge pumping effect [68], might produce a large negative body potential when the switching frequency is very high [57] because the amount of pumped charge is proportional to the switching frequency. Measurements of the body current and potential for various switching frequencies can imply an empirical model for the pumped charge, which, when combined with the I_D-V_B-Q_B relationships in Chapters Four and Five, enables the estimation of SOI circuit speed at very high switching frequencies. A simple way to avoid these detrimental effects is to deplete the film body using the back-gate biasing, such that all the injected electrons are swept to the drain.

Fifth and finally, we recommend design studies of SOI MOSFETs performing under heavy radiation environment. Although the SOI structure is quite insensitive to transient radiation because of the smaller body volume [69-71], and provides latch-up free CMOS, it can be more vulnerable to ionizing total-dose radiation because a conducting channel can be formed at the back surface of the n-channel device, which follows from the positive charge trapping at the back oxide [69-71]. This back-surface conduction, which is significant for SOS n-channel MOSFETs, might be effectively avoided for the SOI MOSFET (shown in Fig. 1.1), by properly biasing the back gate [17,72]. Biasing the back gate at a sufficiently negative voltage will minimize the radiation effects on the n-channel device by not only minimizing the back-gate threshold shift (by pushing the generated holes away from the back $Si-SiO_2$ interface [17]), but also by preventing the additional lowering of the front-gate threshold voltage via the charge-coupling between the two gates [72]. For the SOI CMOS structure in which both p- and n-channel devices have a common back gate, the optimum V_{Gb} with regard to radiation hardness is thus the back-gate threshold voltage of the p-channel device [72]. Radiation effects in 3-D circuits, e.g., stacked CMOS structures [10-16], are subject to further study.

APPENDIX A
POTENTIAL DROP IN SILICON SUBSTRATE

To analyze the effects of the substrate potential drop ψ_{ss} on the $V_{Tf}(V_{Gb})$ characteristic, we express ψ_{ss} in terms of ψ_{sb}, which is known at the onset points of the back-surface inversion and accumulation. The onset points are of interest because V_{Tf} does not vary with V_{Gb} (and hence with ψ_{ss}) when the back surface is either accumulated or inverted.

Applying Gauss' theorem at the substrate-back oxide interface, we have

$$\varepsilon_o E_{ob} = Q_{fs} + Q_{ss} + Q_{cs} + Q_{ds} \qquad (A.1)$$

where Q_{fs} and $Q_{ss} = -C_{ss}\,\psi_{ss}$ are areal densities of the fixed and fast surface-state charges at the substrate-back oxide interface, Q_{cs} is the substrate surface carrier charge density either by inversion or accumulation, and $|Q_{ds}| = [2\varepsilon_s q N_{sub}|\psi_{ss}|]^{1/2}$ is the substrate depletion charge when the substrate has doping density N_{sub}. The electric field at the back oxide $E_{ob}(= \psi_{ob}/t_{ob})$ in (A.1) is also given by combining (2.3) and (2.5) to eliminate E_{sf}:

$$-\varepsilon_o E_{ob} = C_b\psi_{sf} - (C_b + C_{sb})\psi_{sb} + \frac{Q_b}{2} + Q_{fb} + Q_{cb} \quad . \qquad (A.2)$$

Equating (A.1) and (A.2) to remove E_{ob}, we find an expression for ψ_{ss}:

$$C_{ss}\psi_{ss} + [2\varepsilon_s qN_{sub}|\psi_{ss}|]^{1/2} = Q_{fs} + Q_{fb} + Q_{cs} + Q_{cb} + \frac{Q_b}{2} + C_b\psi_{sf} - (C_b + C_{sb})\psi_{sb} \quad . \tag{A.3}$$

For a p-type substrate, the substrate surface is typically inverted due to the large positive Q_{fb} and Q_{fs}. The minimum value of $Q_{fb} + Q_{fs}$ to keep the back surface inverted for the V_{Gb} range of interest, i.e., $V_{Gb}^A < V_{Gb} < V_{Gb}^I$, can be obtained from (A.3) with $\psi_{sf} \simeq \psi_{sb} \simeq 2\phi_B$, $Q_{cb} \simeq Q_{cs} \simeq 0$, and $\psi_{ss} \simeq 2\phi_{B(sub)}$:

$$Q_{fb} + Q_{fs} = C_{sb}2\phi_B + \frac{|Q_b|}{2} + C_{ss}2\phi_{B(sub)} + [2\varepsilon_s qN_{sub}(2\phi_{B(sub)})]^{1/2}. \tag{A.4}$$

For an n-type substrate, the substrate is typically accumulated. The minimum value of $Q_{fs} + Q_{fb}$ to keep the back surface accumulated ($\psi_{ss} \simeq 0$) for $V_{Gb}^A < V_{Gb} < V_{Gb}^I$ is also obtained from (A.3) with the same conditions used in (A.4) but now with $\psi_{ss} \simeq 0$:

$$Q_{fb} + Q_{fs} = C_{sb}2\phi_B + \frac{|Q_b|}{2} \quad . \tag{A.5}$$

APPENDIX B
ACCURACY OF THE SIMPLIFIED DRAIN CURRENT MODEL

The simplified $I_D(V_{Gf},V_{Gb},V_D)$ model developed in Section 3.2 is based on the linear $Q_n(\psi_{sf})$ relationship given by (3.3) and (3.4), which is strictly valid only when the silicon film is completely depleted. If $t_b > x_{d(max)}$, a neutral region can exist near the source. Over this region $Q_n(\psi_{sf})$ is described by the bulk MOSFET theory [32]:

$$\left|Q_n(y)\right| = C_{of}\{V_{Gf} - V_{FB}^f - \psi_{sf}(y) - \frac{1}{C_{of}}[2\varepsilon_s qN_A\psi_{sf}(y)]^{1/2}\} \quad . \tag{B.1}$$

In this Appendix we show that using (3.3) and (3.4) instead of (B.1) results in negligible error in our model for typical SOI MOSFETs.

This error is illustrated in Fig. B.1 where we plot $Q_n(\psi_{sf})$ defined by (B.1) and by (3.3) and (3.4). The curved portion of the plot, which is described by (B.1), depicts the typical case in which $x_{d(max)} < t_b < 2x_{d(max)}$ but the silicon film is completely depleted at the drain. The straight lines follow from (3.3) and (3.4) at the three onset values of V_{Gb} described in Section 3.2. The dashed portions of the lines indicate where discrepancies in $Q_n(\psi_{sf})$ occur. The corresponding error in I_D [described by (3.2)] is proportional to the area between the $Q_n(\psi_{sf})$ curve and the appropriate (depending on V_{Gb}) dashed line. Note that the

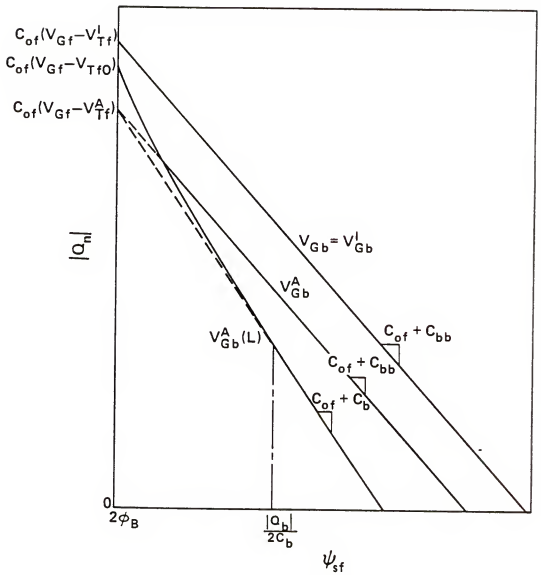

Figure B.1. Illustration of the dependence of Q_n on ψ_{sf}. The curved characteristic is given by (B.1); the straight lines are from (3.3) and (3.4). The slopes of the lines are indicated. The threshold voltages $V^{I}_{Tf} = V^{I}_{FB} + 2\phi_B - Q_b/2C_{of}$ and $V_{TfO} = V^{I}_{FB} + 2\phi_B + qN_A x_{d(max)}/C_{of}$ are described in [32].

error is maximum when the back surface is accumulated everywhere [$V_{Gb} < V_{Gb}^{A}(L)$].

To evaluate this error, we derive more rigorous I_D expression for an SOI MOSFET in which the film body is incompletely depleted near the source. If the complete depletion occurs at $y = y_c$, we can write

$$I_D = \frac{Z}{L}\mu_{nf}\left[\int_{2\phi_B}^{\psi_{sf}(y_c)} |Q_{ni}(y)|d\psi_{sf}(y) + \int_{\psi_{sf}(y_c)}^{2\phi_B+V_D} |Q_{nc}(y)|d\psi_{sf}(y)\right] \qquad (B.2)$$

where $|Q_{ni}(y)|$ and $|Q_{nc}(y)|$, the inversion charge densities at the regions of incomplete and complete film depletion, are given by (B.1) and (3.3) respectively. The $\psi_{sf}(y_c)$ can be obtained from $X_d(y_c) = t_b$:

$$\psi_{sf}(y_c) = \frac{|Q_b|}{2C_b} \quad . \qquad (B.3)$$

Evaluating (B.2) with $V_c \equiv \psi_{sf}(y_c) - \psi_{sf}(0) = |Q_b|/2C_b - 2\phi_B$ yields

$$I_D = \frac{Z}{L}\mu_{nf}C_{of}\left[(V_{Gf} - V_{Tf}^{A})V_D - (1 + \frac{C_b}{C_{of}})\frac{V_D^2}{2} + (\frac{|Q_b|}{2C_{of}} + \frac{C_b}{C_{of}}(2\phi_B + \frac{V_c}{2}))V_c\right.$$

$$\left. - \frac{2}{3}\frac{(2\varepsilon_s qN_A)^{1/2}}{C_{of}}((2\phi_B + V_c)^{3/2} - (2\phi_B)^{3/2})\right] \quad . \qquad (B.4)$$

Note that the last two terms in (B.4) represent the error caused by incomplete film depletion. Since they are bias-independent, the percent error increases with decreasing I_D and reaches the maximum value at $V_{D(sat)} = V_c$: for V_D values smaller than V_c, the film body is not completely depleted anywhere.

We have evaluated this maximum error for $N_A \leq 2 \times 10^{16}$ cm^{-3}, $t_b \leq 1$ μm, and $t_{of} \leq 600$Å. For these ranges of parameter values, which cover most of the contemporary SOI MOSFETs, we found that the error never exceeded about 5% when the silicon film was completely depleted at the drain. The error is smaller for lower N_A and thinner t_{of}. With reference to Fig. B.1, we note that the accuracy of the simplified model is ensured because the slope of the nonlinear $Q_n(\psi_{sf})$ curve $[C_{of} + C_d = C_{of} + (\varepsilon_s q N_A / 2\psi_{sf})^{1/2}]$ does not differ appreciably from $C_{of} + C_b$ for typical devices. Thus the model is sufficiently accurate for all thin-film devices that cannot be modeled as a bulk MOSFET.

APPENDIX C
DEPENDENCE OF CARRIER MOBILITY OF TERMINAL VOLTAGES

For a long-channel MOSFET in which the carrier drift-velocity saturation [67] does not occur, the carrier mobility is mainly degraded by the electric field perpendicular to the channel. Then, at arbitrary position in the channel, the carrier mobility can be characterized empirically as [34]

$$\mu_{nf}(y) = \mu_{max} \left[\frac{E_c}{E_{eff}(y)}\right]^{c_1} \qquad \text{for } E_{eff}(y) > E_c \tag{C.1}$$

where μ_{max}, E_c, and c_1 are fitting parameters that depend on the gate oxidation process and the device properties, and

$$E_{eff}(y) = E_{sf}(y) + \frac{|Q_n(y)|}{2\varepsilon_s} \quad . \tag{C.2}$$

In (C.2), $E_{sf}(y)$ is given by (2.3):

$$E_{sf}(y) = \frac{-Q_b}{2\varepsilon_s} + \frac{\psi_{sf}(y) - \psi_{sb}(y)}{t_b} \quad . \tag{C.3}$$

We consider the following two representative cases. When $V_{Gb} < V_{Gb}^{A}(L)$, the back surface is accumulated throughout the intrinsic device, and with $\psi_{sb}(y) \simeq 0$, (3.3) and (C.3) yield

$$E_{sf}(y) = \frac{C_b}{C_{of}+C_b} \frac{|Q_n(0)| - |Q_n(y)|}{\varepsilon_s} + \frac{|Q_b|}{2\varepsilon_s} + \frac{2\phi_B}{t_b} \quad . \tag{C.4}$$

When $V_{Gb} \simeq V_{Gb}^{I}$, the back surface is completely depleted, and with $Q_{cb}(y) \simeq 0$ in (3.3) and (3.4), (C.3) yields

$$E_{sf}(y) = \frac{C_{bb}}{C_{of}+C_{bb}} \frac{|Q_n(0)| - |Q_n(y)|}{\varepsilon_s} + \frac{|Q_b|}{2\varepsilon_s} \quad . \tag{C.5}$$

Combining (C.1) - (C.5), we can characterize $\mu_{nf}(y)$ in terms of $Q_n(y)$ for the two representative back surface charge conditions.

For the device described in Section 2.4, we plot in Fig. C.1 the measured and calculated linear-region mobility $\mu_{lin}(V_{Gf})$ for $V_{Gb} = 0$ V ($\simeq V_{Gb}^{I}$) and -80 V [$< V_{Gb}^{A}(L)$]. In the calculations we used $Q_n(y) \simeq Q_n(0) \simeq C_{of}(V_{Gf}-V_{Tf})$, and we assumed an average value $N_A = 10^{16}$ cm^{-3} for the nonuniform doping density. The fitting parameters $\mu_{max} = 420$ cm^2/V-sec, $c_1 = 0.4$, and $E_c = 1.25 \times 10^5$ V/cm in (C.1) were determined from the log-log plot of the measured μ_{lin} versus the calculated E_{eff}. We see good agreement in Fig. C.1 between the measured and calculated plots when $V_{Gf} > 2$ V where the effects of grain boundaries in the film have negligible effects. Note that μ_{lin} is virtually independent of V_{Gb} because E_{sf} in (C.4) and (C.5), which

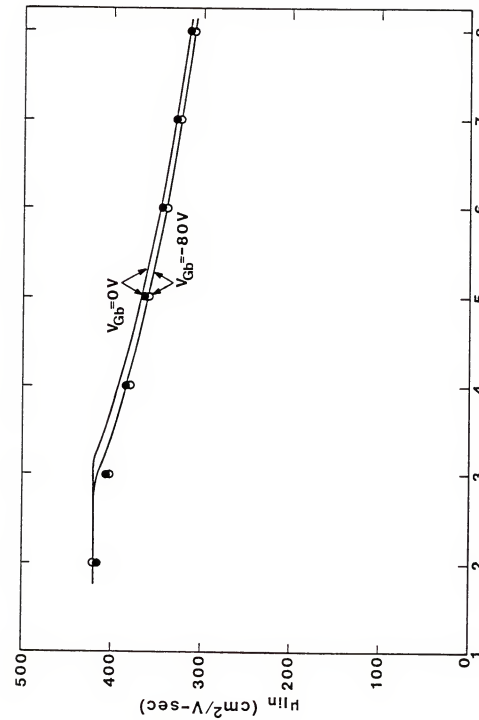

Figure C.1. Measured (points) and calculated (curves) linear-region (electron) mobilitiy versus the gate voltages of the SOI MOSFET. The measured values were obtained from the $I_D(V_{Gf})$ characteristic at V_D = 50 mV.

conveys the main V_{Gb} dependence, is low and hence does not strongly affect E_{eff}.

For high V_D however, $E_{sf}(y)$ is high near the drain, and its strong dependence on V_{Gb} is thus reflected by $E_{eff}(y)$ and $\mu_{nf}(y)$. We plot in Fig. C.2 the calculated $\mu_{nf}(y)/\mu_{max}$ of the measured device in the saturation region for V_{Gf} = 8 V and V_{Gb} = 0 V and -80 V. The same fitting parameters and $Q_n(y) = Q_n(0)(1-y/L)^{1/2}$, which we derive in Appendix D, were used in the calculations. Unweighted averaging across the channel of $\mu_{nf}(y)$ in Fig. C.2 defines the effective mobility μ_{sat} ($I_{D(sat)} \propto \mu_{sat}$) and its appreciable dependence on V_{Gb}. Note that this dependence is due mainly to the influence of V_{Gb} on $\mu_{nf}(y)$ near the drain.

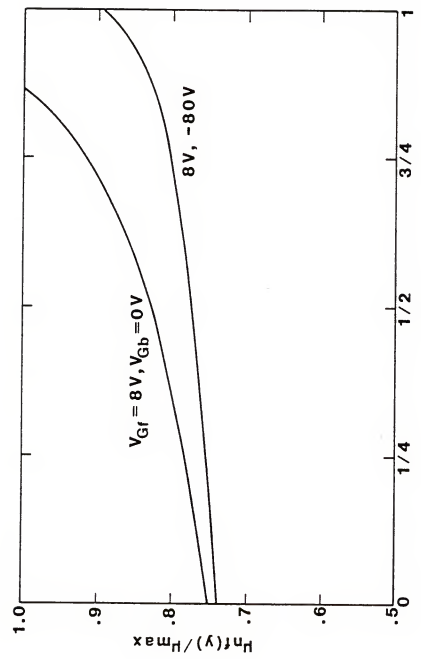

Figure C.2. Calculated mobility variation along the channel of the saturated device at V_{Gf} = 8 V and V_{Gb} = 0 V and -80 V. The maximum mobility $\mu_{max} \approx 420$ cm^2/V-sec obtains at low V_{Gf} as shown in Fig. C.1.

APPENDIX D
DERIVATION OF THE POSITION DEPENDENCES OF THE INVERSION CHARGE DENSITY AND SURFACE POTENTIAL

For a strongly inverted n-channel MOSFET, the current in the (front) channel $(0 \leq y \leq L)$ is [32]

$$I(y) = Z \mu_n |Q_n(y)| \frac{d\psi_{sf}(y)}{dy} \quad . \tag{D.1}$$

The linearity of $Q_n(\psi_{sf})$ in (3.3) and (3.4) can be expressed as

$$\frac{d|Q_n(y)|}{d\psi_{sf}(y)} = C_{of} + C_{body} \tag{D.2}$$

where the body capacitance C_{body} is dependent on the charge condition at the back surface. When the back surface is accumulated, $\psi_{sb}(y)$ does not vary appreciably along the channel. Then (3.3) and (D.2) yield

$$C_{body} = C_b \quad . \tag{D.3}$$

When the back surface is depleted, $\psi_{sb}(y)$ can vary. Thus combining (3.3) and (3.4) to remove $\psi_{sb}(y)$, and noting that $Q_{cb}(y) \approx 0$, we find

$$C_{body} = C_{bb} \triangleq \frac{C_{ob}C_b}{C_{ob}+C_b} \quad . \tag{D.4}$$

Combining (D.1) and (D.2) and integrating (D.1) from the source (y=0) to arbitrary y, we get

$$I(y) = \frac{Z}{y}\,\mu_n\,\frac{Q_n^2(0)-Q_n^2(y)}{2(C_{of}+C_{body})} \quad . \tag{D.5}$$

Recognizing that I(y) = I(L) in the quasi-steady-state, we rewrite (D.5) as

$$Q_n(y) = Q_n(0)\left[1 - \frac{y}{L} + \left(\frac{Q_n(L)}{Q_n(0)}\right)^2 \frac{y}{L}\right]^{1/2} \quad . \tag{D.6}$$

The $\psi_{sf}(y)$ dependence can now be obtained by integrating (D.2) from the source to arbitrary y. With $\psi_{sf}(0) = 2\phi_B$, which follows from the strong-inversion approximation [32], we get

$$\psi_{sf}(y) = 2\phi_B + \frac{Q_n(y)-Q_n(0)}{C_{of}(1+\alpha)} \tag{D.7}$$

where

$$\alpha \triangleq \frac{C_{body}}{C_{of}} \quad , \tag{D.8}$$

which varies with the back-surface charge condition because C_{body} does as indicated in (D.3) and (D.4).

To describe $Q_n(y)$ and $\psi_{sf}(y)$ in terms of the terminal voltages and V_B, we derive the expressions for $Q_n(0)$ and $Q_n(L)$. From (3.3) and (3.4) we can easily show that $Q_n(0)$ has the general form

$$Q_n(0) = -C_{of}(V_{Gf} - V_{Tf}) \tag{D.9}$$

where V_{Tf} is the (front-gate) threshold voltage, given by (4.2)and (2.12) when the back surface is accumulated and depleted respectively

When the device is saturated $Q_n(L) \cong 0$. In the triode region, $Q_n(L)$ is obtained by combining (D.7), (D.9), and $\psi_{sf}(L) = 2\phi_B + V_D$:

$$Q_n(L) = -C_{of}[V_{Gf} - V_{Tf} - (1 + \alpha)V_D] \quad . \tag{D.10}$$

The saturation thus occurs at

$$V_D = V_{D(sat)} \cong \frac{V_{Gf} - V_{Tf}}{1 + \alpha} \quad . \tag{D.11}$$

Note that the derived expressions for $Q_n(y)$ and $\psi_{sf}(y)$ given by (D.6) - (D.11) are valid for the both back-surface charge conditions if α and V_{Tf} are evaluated accordingly. In fact, these descriptions of $Q_n(y)$ and $\psi_{sf}(y)$ are generally valid for any MOSFET in which $Q_n(\psi_{sf})$ is linear, i.e., α is independent of V_D.

APPENDIX E
SIGNIFICANCE OF THE TRANSIENT TRANSPORT CURRENT

To investigate the effects of I_{TT} on the transient analysis of MOS circuits, we evaluate Q_{TT}, the amount of source-drain transport charge carried by I_{TT} during an OFF-ON switching transient. When the device is turned from a steady-OFF-state ($t = t_o$, $V_{GfS} < V_{Tf}$) to a steady-ON-state ($t = t_1$, $V_{GfS} = V_{DD}$), (5.34) gives

$$Q_{TT} = \int_{t_o}^{t_1} I_{TT}\, dt = \int_{0}^{V_{DD}-V_{Tf}} C_{TT}\, d(V_{GfS} - V_{Tf}) \tag{E.1}$$

if V_{DS} is fixed. Note that Q_{TT} is independent of the rise time of the gate pulse. If $V_{DS} > (V_{DD} - V_{Tf})/(1 + \alpha)$, (D.11) implies that the device is in the saturation region throughout the turn-on transient. Then (E.1), with (5.35) in which $u = 1$, yields

$$Q_{TT} = Q_{TT(sat)} = -ZLC_{of}(V_{DD} - V_{Tf})\left(\frac{4}{15}\right) \equiv \frac{2}{5} Q_N \tag{E.2}$$

where Q_N is given in (5.7.b) or (5.12.b). If $V_{DS} < (V_{DD} - V_{Tf})/(1 + \alpha)$, the device moves to the triode region from the saturation region as V_{GfS} increases, and

$$Q_{TT} = -ZLC_{of}(V_{DD} - V_{Tf})\left[\frac{1}{4u} + \frac{1}{60u(2u-1)^2} + \frac{\ln(2u-1)}{6u}\right] \quad . \qquad (E.3)$$

As expected, Q_{TT} is identical to the discrepancy between Q_D in (5.18.b) and the electrostatically predicted drain charge [37,38]. For example, when the device is saturated, since the channel charge is independent of V_D, the electrostatic Q_D is zero, whereas it is $(2/5)Q_N$ in our model, which is identical to Q_{TT} in (E.2). When V_{DS} is near zero (linear region), $Q_D \approx Q_N/2$ in both models, and $Q_{TT} \approx 0$.

Another insightful result that follows from I_{TT} is the average time lag $\bar{\tau}_D$ in the actual saturation drain current, behind the quasi-static I_o, during the turn-ON. This delay is defined by

$$I_{D(sat)}(t) = I_o(t - \bar{\tau}_D) \quad . \qquad (E.4)$$

We therefore can write, independent of the rise time of $I_o(t)$,

$$\bar{\tau}_D I_{DD} = \int_{t_o}^{t_1} [I_o(t) - I_{D(sat)}(t)]\, dt \qquad (E.5)$$

where I_{DD} is the quasi-static current in the steady-ON-state at $V_{GfS} = V_{DD}$. Since $C_{GfD} = C_{GbD} = 0$ in the saturation region, $I_{D(sat)}(t)$ is identical to the transport current $(I_o + I_{TT})$. Hence the integrand in (E.5) is $I_{TT}(t)$, and

$$\bar{\tau}_D I_{DD} = Q_{TT(sat)} \quad . \qquad (E.6)$$

Using the expression for I_{DD} derived from (D.11) and (5.17) and the expression for $Q_{TT(sat)}$ in (E.2), we get

$$\bar{\tau}_D = \frac{8}{15} \tau_o \tag{E.7}$$

where

$$\tau_o = (1 + \alpha) \frac{L^2}{\mu_n (V_{DD} - V_{Tf})} \quad . \tag{E.8}$$

Note that this result is consistent with previous work [52,53]: $\bar{\tau}_D$ is slightly longer than the minimum carrier transit time after abrupt turn-ON, calculated by Burns ($0.38\ \tau_o$) [52] and by Oh, et al. ($0.5\ \tau_o$) [53].

These simple expressions for Q_{TT} and $\bar{\tau}_D$ are useful in assessing the significance of finite carrier transit delay on the charge conservation and circuit delay in MOS circuits. The I_{TT} in the equivalent circuit might not be important for the bulk MOS circuits in which the extrinsic capacitances are predominant. However for SOI MOS circuits in which the parasitic capacitances in the extrinsic part of the device are small, neglecting I_{TT}, i.e., Q_{TT} and $\bar{\tau}_D$, like in the conventional reciprocal-capacitance model [30,40], might result in a significant charge nonconservation as well as an underestimation of circuit delay.

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BIOGRAPHICAL SKETCH

Hyung-Kyu Lim was born in Kyung-Nam, Korea, on February 4, 1953. He received the B.S. degree in electronic engineering from the Seoul National University in 1976 and the M.S. degree in electrical engineering from the Korea Advanced Institute of Science, Seoul, Korea, in 1978. Since August 1981, he has been working toward the Ph.D. degree at the University of Florida, Gainesville.

From 1978 to 1981 he was with Samsung Semiconductor Inc., Bucheon, Korea, where he was engaged in the development of MOS and bipolar integrated circuits, particularly low-power CMOS circuits.

His area of interest includes high-speed, high-density MOS device structures and modeling.

He is a member of IEEE and Tau Beta Pi.

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Jerry G. Fossum, Chairman
Professor of Electrical Engineering

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Fredrik A. Lindholm
Professor of Electrical Engineering

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Sheng S. Li
Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Dorothea E. Burk
Assistant Professor of Electrical Engineering

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Timothy J. Anderson
Associate Professor of Chemical Engineering

This dissertation was submitted to the Graduate Faculty of the College of Engineering and to the Graduate Council, and was accepted as partial fulfillment of the requirements for the degree of Doctor of Philosophy.

August 1984

Hubert A. Beve

Dean, College of Engineering

Dean for Graduate Studies and Research